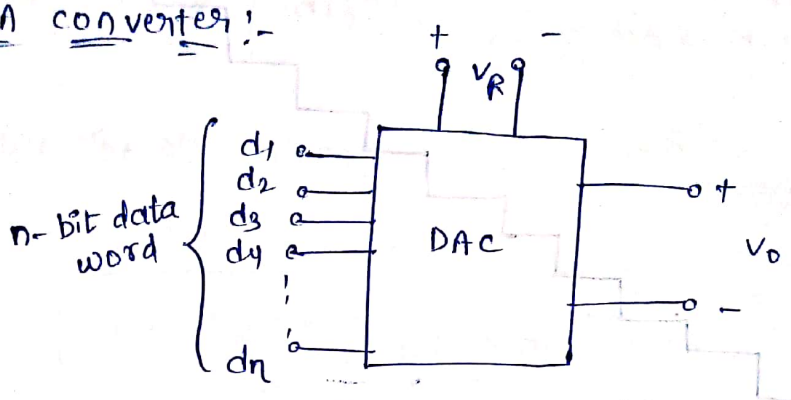
Unit-6

Analog to Digital & Digital to Analog converters

D-A converter :-



$$V_o = kV_{FS}\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right)$$

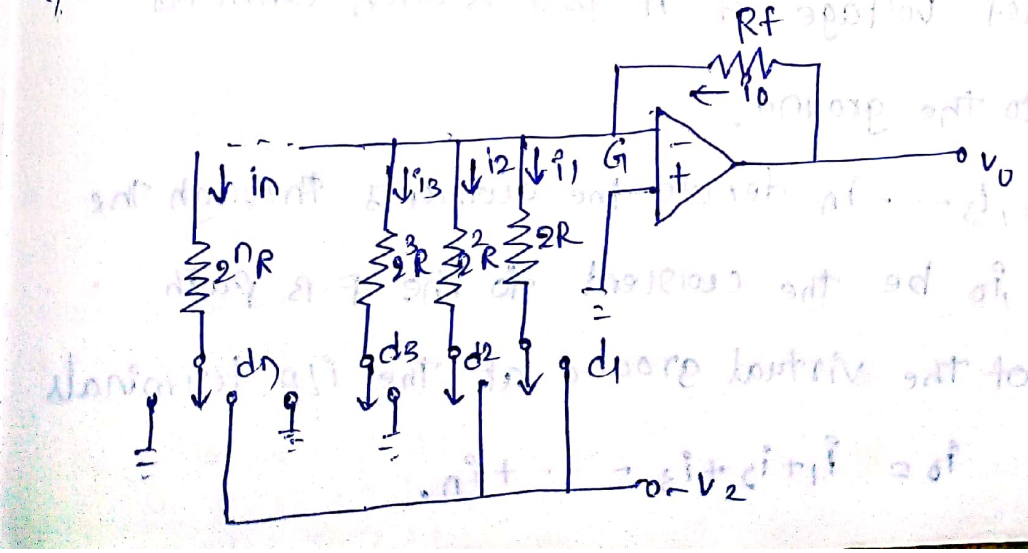
where, k is scaling factor which is usually unity

V_{FS} fullscale o/p voltage d_1 is the most significant bit with a weight of $V_{FS}/2$. D_n is least significant bit with a weight of $V_{FS}/2^n$.

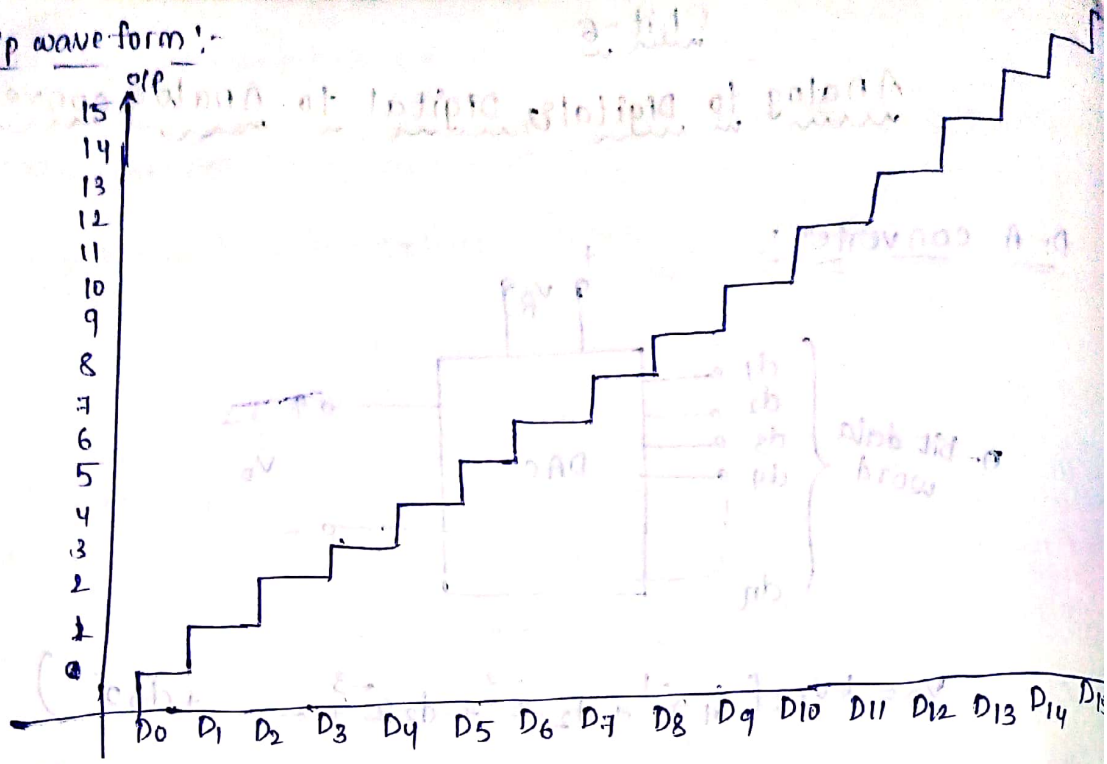
→ D-A converters are basically 3 types;

1. Binary weighted resistor.
2. R-2R ladder
3. inverter R-2R.

Binary weighted resistor D-AC :-



O/p wave form :-



→ A binary weighted resistor is diagramatically represented as shown in fig

→ from the fig an op amp uses a set of weighted resistors $2R, 2^2R, 2^3R \cdots 2^nR$. connected to a set of switches as shown in fig

→ $d_1, d_2, d_3 \cdots d_n$ are n electronic switches controlled by the binary i/p word they are single pole, double through switches.

→ If the binary i/p is 1 it connects the resistance through ref voltage if it is 0 switch connects resistor to the ground.

→ let $i_1, i_2, i_3 \cdots i_n$ denote the currents through the resistors, i_0 be the current to the F.B path. because of the virtual ground at the i/p terminals we have $i_0 = i_1 + i_2 + i_3 \cdots + i_n$.

$$i_0 = -\left[\frac{V_R}{2R}d_1 + \frac{V_R}{2^2R}d_2 + \frac{V_R}{2^3R}d_3 + \cdots + \frac{V_n}{2^nR}d_n\right]$$

$$i_0 = -\frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots d_n 2^{-n}\right]$$

→ But the o/p voltage

$$V_0 = -i_0 R_f$$

$$\boxed{V_0 = \frac{V_R R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]}$$

→ Then compare to the general eqn the scaling factor 'k' becomes '1' and full scale voltage is equal to ref voltage.

$$\therefore V_0 = V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

→ let the i/p be a 4 bit binary word

$$D = d_1, d_2, d_3, d_4$$

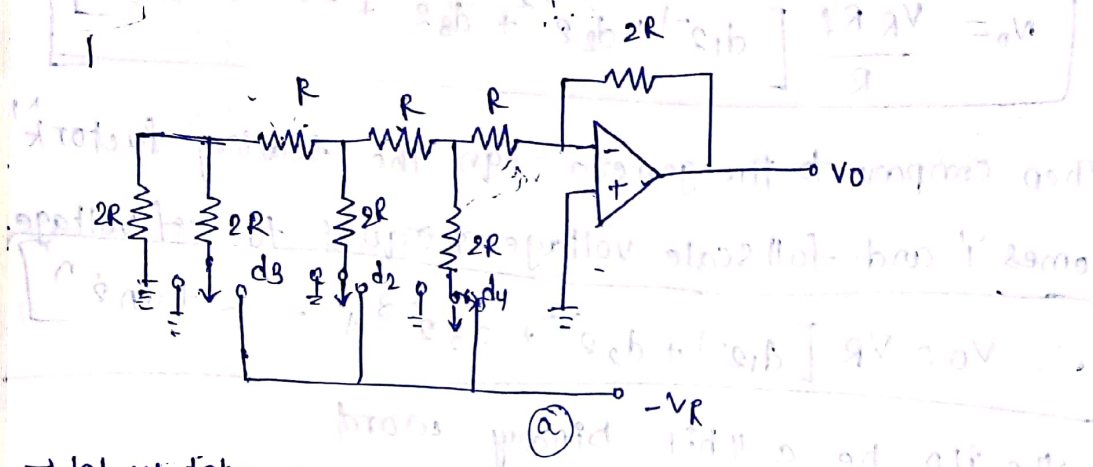
Since for $n=4$ the no. of digital i/ps is possible is $2^4 = 16$.

	d_1	d_2	d_3	d_4
D_0	0	0	0	0
D_1	0	0	0	1
D_2	0	0	1	0
D_3	0	0	1	1
D_4	0	1	0	0
D_5	0	1	0	1
D_6	0	1	1	0
D_7	0	1	1	1
D_8	1	0	0	0
D_9	1	0	0	1
D_{10}	1	0	1	0
D_{11}	1	0	1	1
D_{12}	1	1	0	0
D_{13}	1	1	0	1
D_{14}	1	1	1	0
D_{15}	1	1	1	1

→ the graphical representation of analog o/p voltag V_0 agai all possible i/p words is shocon in fig from the fig it is seen that the analog o/p voltage is a +ve staircase the o/p is +ve.

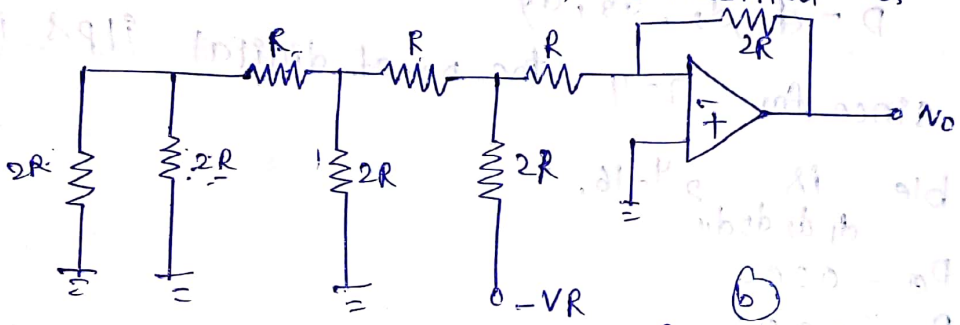
→ since the ref voltage is -ve.

R-2R ladder DAC :-

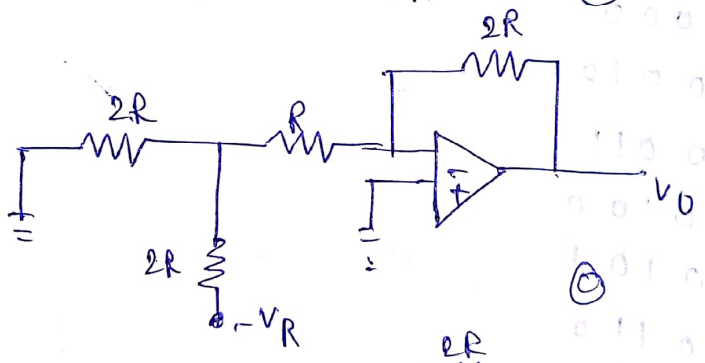


(a)

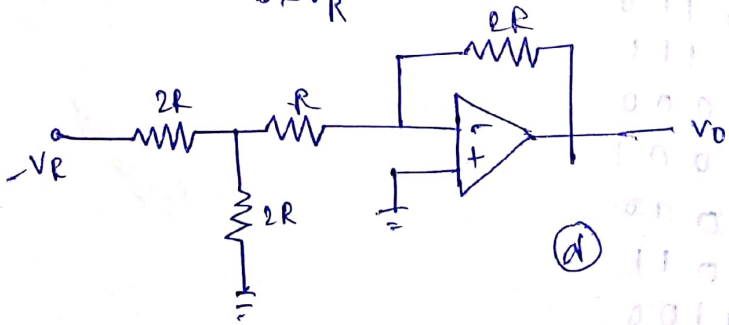
→ let us take D = 100 the ckt can be modified as



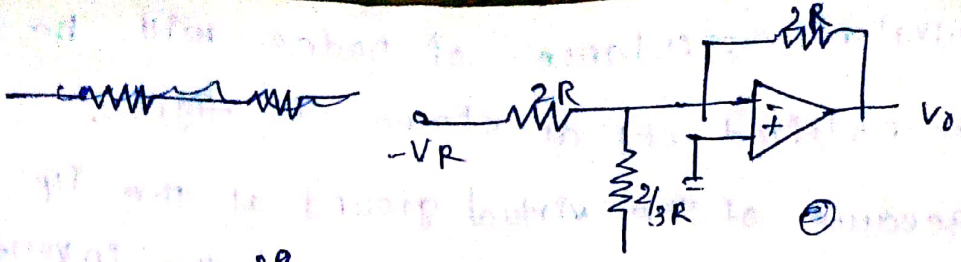
(b)



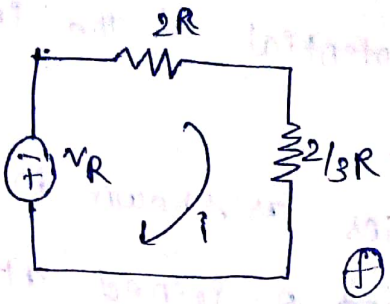
(c)



(d)



(e)



(f)

→ This type of DAC uses only two values of resistors and hence it is easy to fabricate all resistors on a chip. The usual values of the resistors range from 2.5kΩ to 20kΩ. The resistors are (R-2R) so arranged as to form a ladder n/w as shown in fig.

→ The analog voltage o/p for any binary i/p can be determined as follows.

→ Let the digital i/p be a 3-bit binary word given as D = 100 ; $d_1 = 1$, $d_2 = 0$ and $d_3 = 0$. The switch positions are shown arrow.

→ The ckt is redrawn below (b)

To find the voltage at node-3 i.e, v_3 from the ckt.

i) $2R // 2R = \frac{2R \times 2R}{2R+2R} = \frac{4R^2}{4R} = R$.

ii) $R + R = 2R$

iii) $2R // 2R = \frac{2R \times 2R}{2R+2R} = \frac{4R^2}{4R} = R$

iv) $R + R = 2R$.

equivalent resistance of nodes will be 2R.

The modified ckt as shown in fig (c).

→ Because of the virtual ground at the i/p terminals of the op-amp, the potential of the inverting i/p terminal is also zero.

→ The ckt further modifies as shown in fig.

Both resistors 2R and R joined at node 3 are at zero potential. They can be replaced by a single resistance.

→ from fig (d)

$$2R//R = \frac{2R \times R}{2R+R} = \frac{2R^2}{3R} = 2/3R.$$

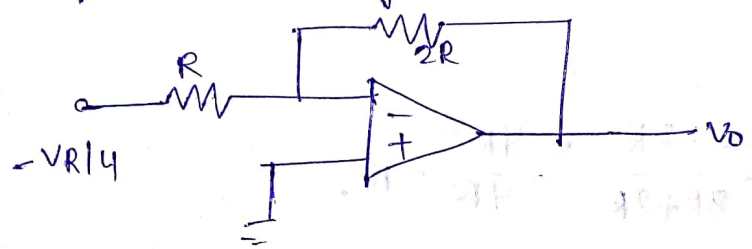
→ The ckt (d) further modifies as shown ckt (e)

$$i = \frac{-V_R}{2R + 2/3R} = \frac{-3V_R}{8R}$$

$$V_3 = \frac{2R}{3}\left(\frac{-3V_R}{8R}\right) = \frac{-V_R}{4}$$

Hence the potential at node 3 $= -V_R/4$

→ The original ckt may be redrawn as follows.



we have closed loop gain $\frac{V_o}{V_i} = 2$

But $V_i' = -V_R/4$

o/p voltage $V_o = -2(-V_R/4) = \frac{V_R}{2} = V_{FS}/2$

$$\boxed{V_o = V_{FS}/2}$$

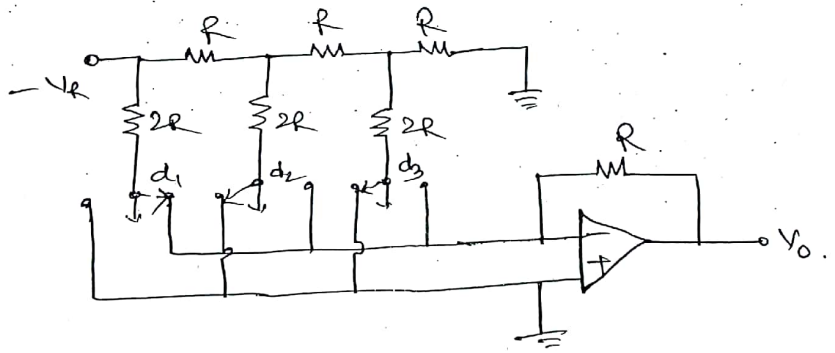
$\therefore V_R = V_{FS}$

Inverted R-2R ladder DAC.

In the R-2R ladder DAC, current in every one of the resistors changes, as and when the input data change. An increase of current results in more heat being general and thus there is a larger dissipation of power. This is highly undesirable in practice.

This drawback is overcome in the inverted R-2R ladder DAC.

An inverted R-2R ladder DAC with a 3-bit input is shown in fig.



d_1 ... MSB
d_3 ... LSB.

It may be observed that the positions of MSB and LSB are interchanged. Compare with the R-2R ladder DAC. The arrangement of switches is such that the input binary word connects the switches to either the ground or inverting input terminal. But the inverting input terminal is also at ground potential because of virtual ground. This makes the current in the resistances to be the same,

Independent of the input.

Let the input binary word be D = 001.

The positions of the switches are shown dotted.

Since the current through each branch of the Ladder network is constant, the voltages of the nodes remain constant at $\frac{V_R}{2^0}$, $\frac{V_R}{2^1}$, $\frac{V_R}{2^2}$.

Analog-to-Digital converters (ADC) :-

A practical analog-to-digital converter accepts an analog input voltage and produces an output binary word $d_1 d_2 d_3 ---- d_n$ of functional value D, such that $D = d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + ---- + d_n 2^{-n}$

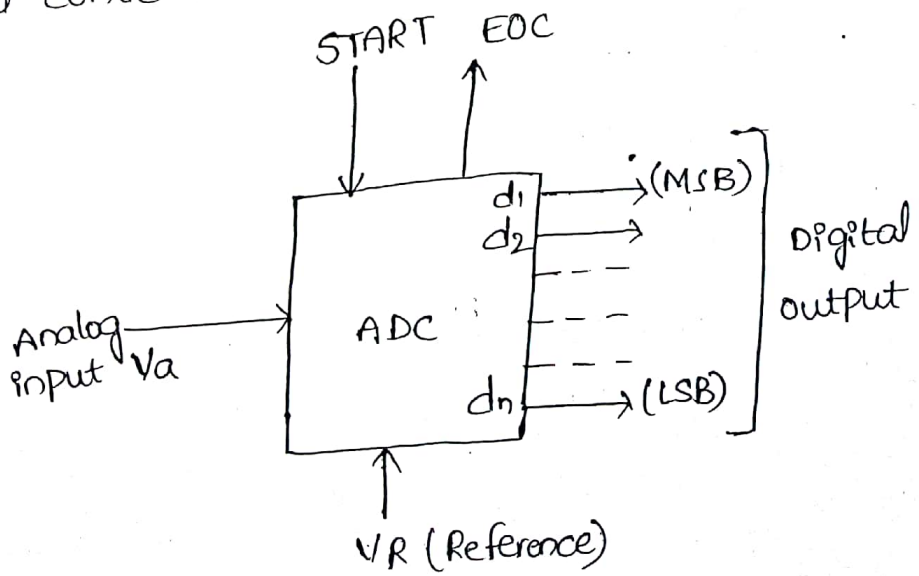
In the above expression for D, d_1 is the most significant bit (MSB) and d_n is the least significant bit (LSB)

There are two additional control lines in an ADC: the START and EOC

The START input tells the converter when precisely to start the conversion, and the EOC (end of conversion) output announces when the conversion is complete.

A to D converters are either interfaced with microprocessor or they drive directly LCD or LED displays

It is a block diagram representation of an analog-to-digital converter.



classification of ADC's :-

Based upon the technique adopted for conversion, analog-to-Digital converters are broadly classified into two groups.

(i) Direct type ADC's and

(ii) Integrating type ADC's.

A direct type ADC compares a given analog input signal with an internally generated equivalent signal, whereas an integrating type ADC does the conversion in an indirect manner. The analog input signal is first converted into a linear function of frequency or time, and this is subsequently converted into a digital code.

Some of the direct type ADC's are

(i) Flash converter (or parallel comparator ADC)

(ii) Counter type converter (or ADC using DAC)

(iii) Tracking or servo meter

(iv) Successive approximation type converter etc.

Integrating type converters which find wide application in practice are:

(i) charge balancing ADC and

(ii) Dual slope ADC.

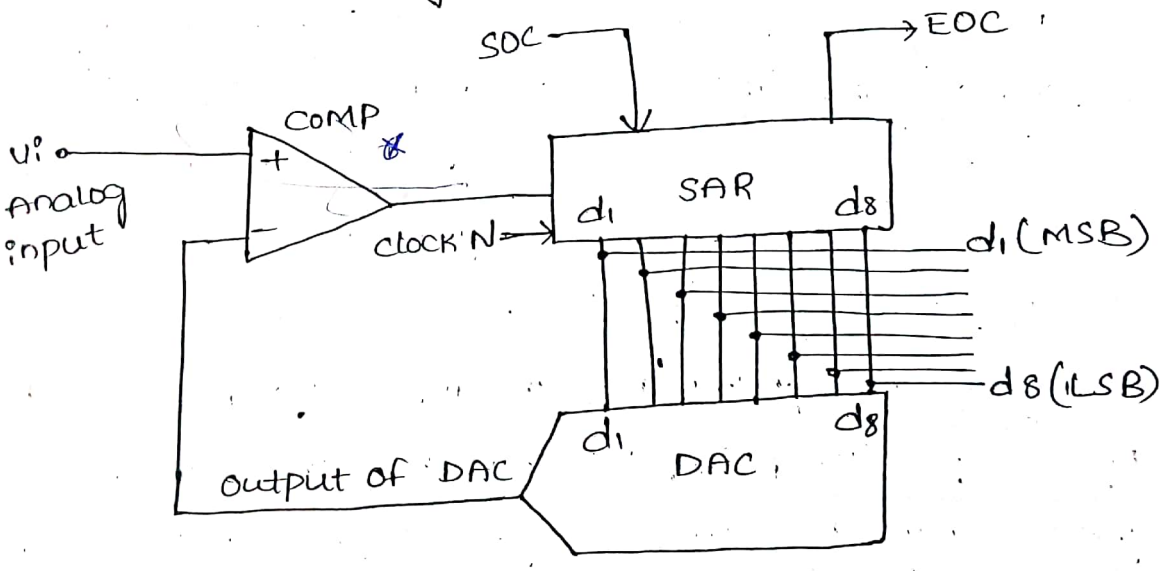
binary search.

The searching process is very fast, a n-bit conversion being completed in only n clock periods.

The strategy consists in adjusting the i/p code of DAC such that its outputs is within = $\pm \frac{1}{2}$ LSB of the analog input signal.

which is to be converted into equivalent digital signal it is a trial and error process. and that particular code which comes nearest is the required ADC output

The block diagram a successive approximation ADC is as shown in figure



SOC. Start of conversion ; EOC. End of conversion

The ckt uses a successive approximation register, a DAC and a comparator.

The external clock input sets the internal timing

end of the conversion process.

Operation:-

As already seen, the basic idea of using a SAR is to find, by trial and error process, the required value of each bit of the digital output. the operation takes place as follows.

The SOC signal initiates the process of search. the SAR sets the MSB (most significant bit) $d_1=1$, as soon as the START signal arrives, and all other bits are set to 0. If the converter is a 8-bit converter, the initial setting would be, 10000000. The output V_d of the DAC for this trial code is compared with the analog input V_i

If the analog i/p V_i is greater than the DAC output V_d it implies that the trail code 10000000 is less than the correct digital representation of V_i the MSB d_1 is left at 1 and the next lower significant bit is set at 1, and the process is repeated.

If, on the other hand, the input V_i is less than the DAC output V_d, it implies that the trail code 10000000 is greater than the correct digital representation of V_i in such an event, the MSB is set to 0, and the next lower significant bit is set to 1, and the process is repeated.

Thus the above process of comparision is repeated for all subsequent bits, one ata time, untill all bit positions have been tested.

The comparator changes state whenever the DAC output crosses V_i and this activates the EOC (end of conversion) command.

It is seen that with the successive comparison of the bits DAC output, the output voltage of the ADC becomes more and more close to the actual analog input voltage

Whatever the value of the analog input, only eight pulses are required to establish the accurate output.

In practice, however, an additional pulse is needed to load the output register and reinitialize the ckt

A typical conversion sequence is given in figure.

correct digital representation	SAR o/p V_A at different stages	comparator output
1 0 1 1 0 0 1 0	1 0 0 0 0 0 0 0	1
	1 0 1 0 0 0 0 0	0
	1 0 1 0 0 0 0 0	1
	1 0 1 1 0 0 0 0	1
	1 0 1 1 1 0 0 0	0
	1 0 1 1 0 1 0 0	0
	1 0 1 1 0 0 1 0	1
	1 0 1 1 0 0 1 1	0

Comparator o/p after comparing all 8-bits = 10110010 = digital representation of analog i/p.

The time required for one conversion from analog to digital depends on both the clock period T and no. of bits n. Let T_c denote the conversion time

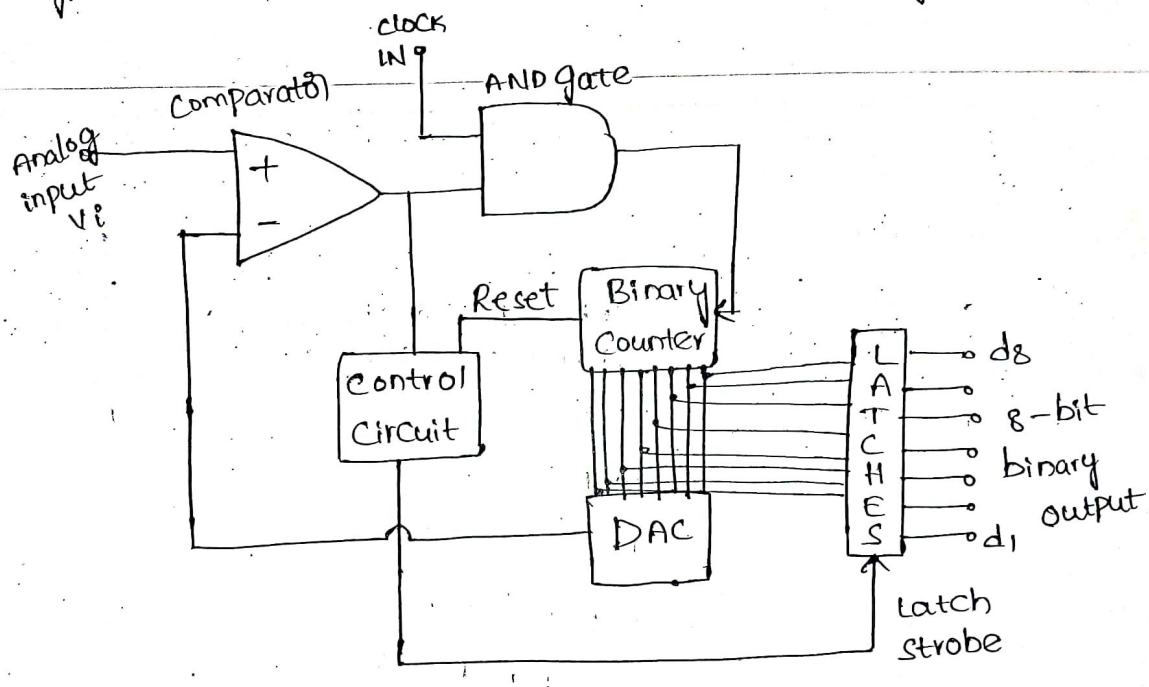
We have $T_c = T(n+1)$

$V_0 = -V_i$ (or) $V_0 = V_i$

Counter type ADC (or ADC using DAC)

The Counter type ADC is also referred to ADC using DAC since the circuit uses a DAC. The basic principle employed in this type of ADC is that the linear ramp can be produced by connecting the output of a counter to the input of a DAC

The block diagram representation of a counter type A to D converter is as shown in figure



Operation:—

The binary counter is reset to zero. The o/p of DAC is also zero. The analog i/p voltage is applied at the non inverting (+) input terminal of the Comparator As studied earlier since the i/p voltage is more possitive the comparator o/p goes high. this enables the AND gate and the clock reaches out to the counter. The counter begins to count the clock pulses. each clock

pulse increases the o/p voltage of the DAC by one step. the result is that a stair case voltage is generated at the o/p of the DAC. if the no. of steps of the stair case is quite large, the o/p voltage may be approximated to a linear ramp.

As soon as the DAC o/p voltage exceeds the applied i/p voltage the comparator output goes low. This disables the AND gate with the result that the clock gets disconnected from the counter.

The control circuitry of the device provides a latch strobe. The counter output is latched. Also the counter gets reset to zero device.

The latched data is displayed by using decoder and display device.

Thus Analog-to-digital conversion is achieved.

The counter type DAC also suffers from certain drawbacks.

(i) the speed is comparitively low.

(ii) the DAC used must be precise and sensitive

(iii) if the i/p signal is time-varying, it needs to be sampled by means of a sample and hold circuit, before it is applied to the comparator

Dual slope DAC :-

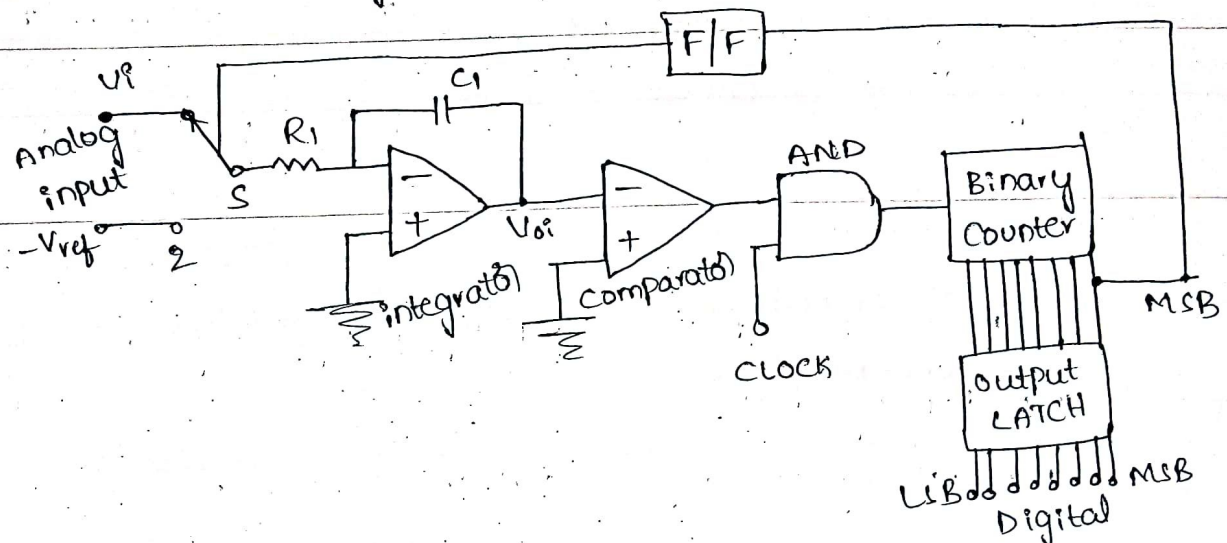
The dual slope DAC is an integrator type D. to A converter. its accuracy is quite high, even though the speed of operation is quite low.

using an o/p voltage [illegible] i/p signals conduction

In the circuit uses an integrator and a flip in addition to a comparator and binary counter

In the dual slope DAC, the analog i/p voltage and a reference voltage are both converted into time periods by means of an integrator, and are then measured by means of a counter

The block diagram representation as shown in fig



The integrator is a ramp generator. there is a switch arrangement S by which the integrator input can be switched b/w the analog i/p voltage Vi and a negative reference voltage -Vref The switch is controlled by the MSB of the binary counter (see blocks diagram)

when the MSB is a logic 0, the switch closes on terminal 1 at which the i/p voltage is applied.

when the MSB is a logic 1, the switch closes on terminal 2 at which the reference voltage is applied

Operation :-

Let the analog switch close on terminal 1 at t = 0. The analog i/p voltage Vi gets applied at the inverting terminal of the integrator

The integrator o/p voltage is given as

$$V_{oi} = -\frac{1}{R_1 C_1}\int_0^{t_1} V_i dt$$

$$= -\frac{V_i t_1}{R_1 C_1}, \text{ if } V_i \text{ is assumed to be constant over the interval } 0 \text{ to } T_1.$$

The integrator o/p voltage is applied to the comparator. The comparator output goes high, it enables the AND gate and the clock pulses reach the counter.

At the end of 2^n clock periods, the MSB of the counter goes high. This causes the output of the flip-flop to go high with the result that the analog switch S switches from position 1 to position 2, and connects the reference voltage to the integrator inverting terminal.

Simultaneously the binary counter gets reset. The neagative reference voltage $-V_R$ which now forms the i/p to the integrator makes the o/p of the integrator increase as a positive linear ramp. when it reaches zero level, the comparator o/p goes low and this disables the AND gate,

takes place and ... half ...

and the result of it is that the clock pu... cease to reach the counter. The counter stops at a count corresponding a time interval t_2.

Since the integrator o/p voltage, originally zero drops to a definite voltage V in time t_1, and rises to the original voltage Vi. Viz

zero in time t_2, we have

Charge voltage = Discharge voltage

$$\therefore \frac{V_i t}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

Or $V_i t_1 = V_R t_2$ or $t_2 = \frac{V_i t_1}{V_R}$

In the above expression for t_2, V_R and t_1 are fixed. Hence $\boxed{t_2 \propto V_i}$

That is, t_2 is directly propotional to the analog i/p voltage and hence is measure of it. The o/p of the counter is a binary number which corresponds to time t_2.

Thus the binary digital o/p of the counter is also propotional to the analog input.

We have digital o/p of the counter = (Counts/sec) t_2

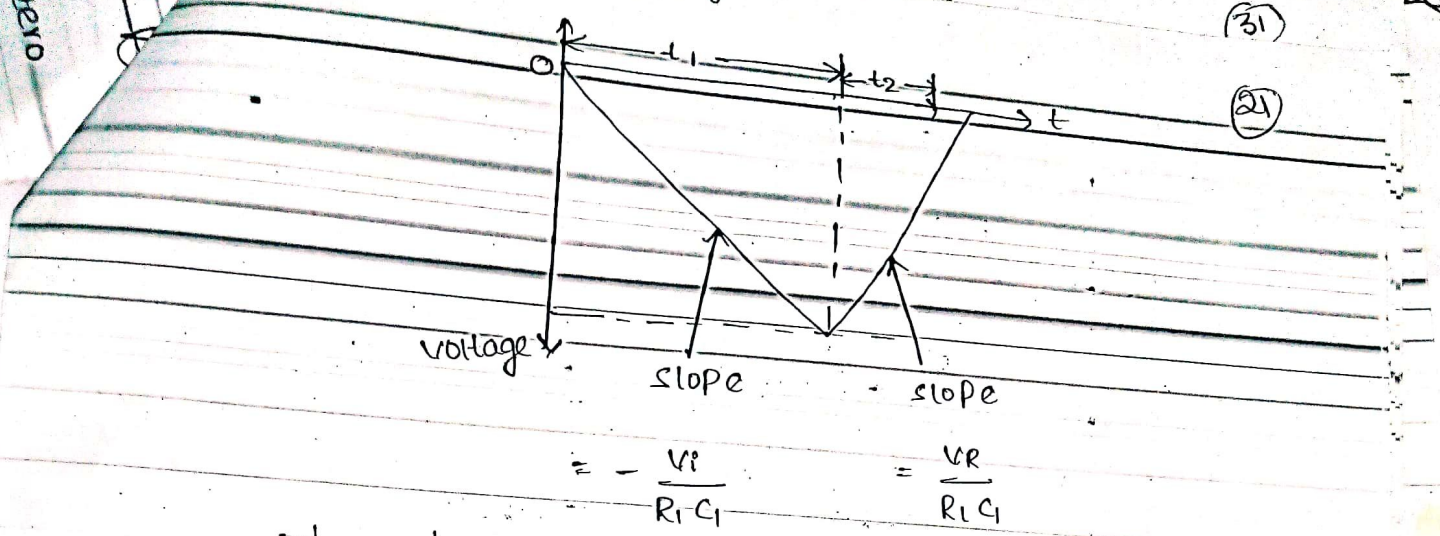
But $t_2 = \frac{V_i t_1}{V_R}$

$\therefore$ Digital o/p of the Counter = (Counts/sec) $t_1 \left(\frac{V_i}{V_R}\right)$

The counter o/p is displayed suitably.

The wave form of the integrator o/p voltage

conduction is as shown in figure



$$= -\frac{V_i}{R_1 C_1} \qquad = \frac{V_R}{R_1 C_1}$$

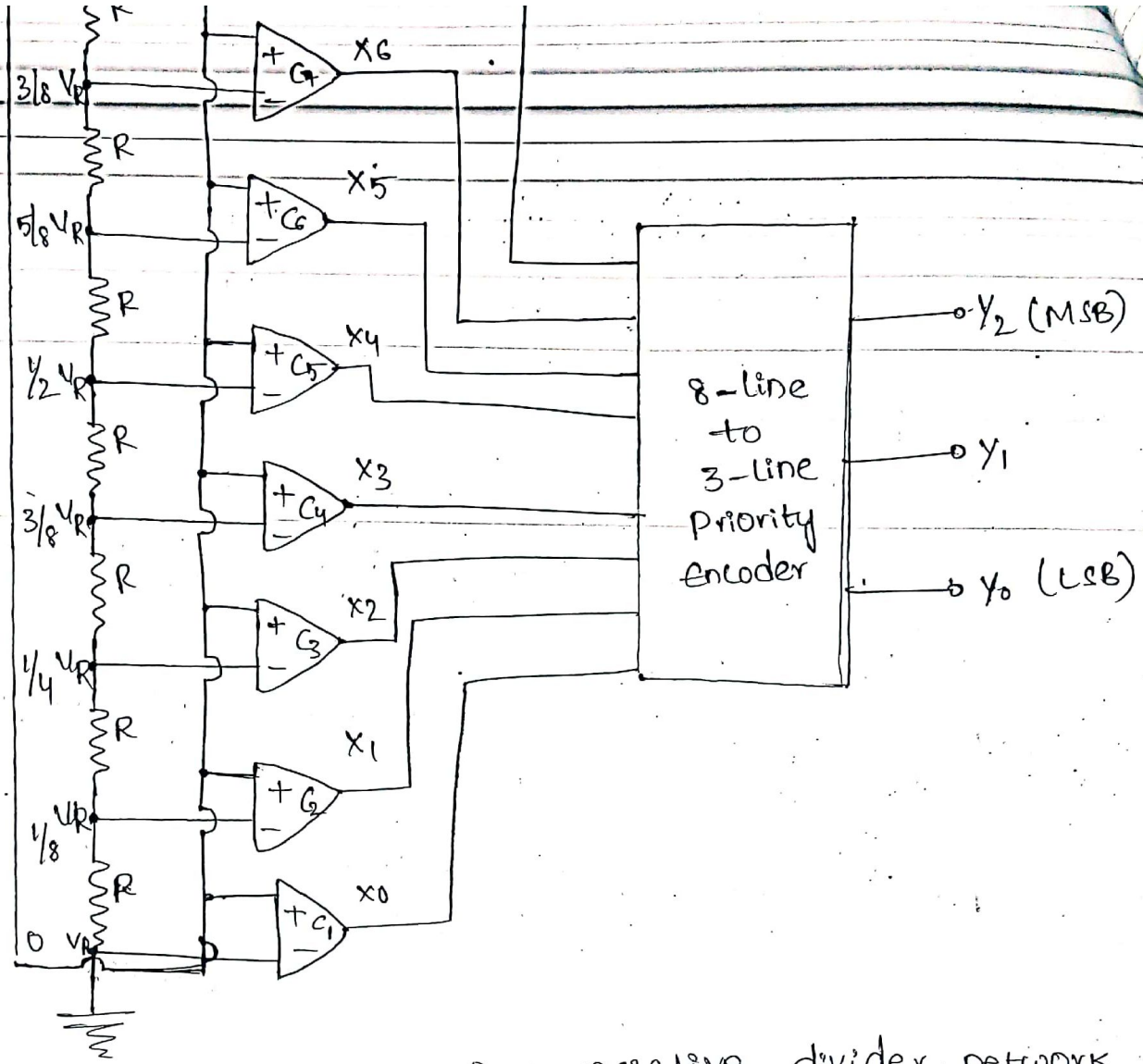
The dual slope ADC is very widely used in Practice in view of its many adiantages

(i) It possesses a high degree of accuracy
(ii) It is cheap and
(iii) Its Performance is not adversely affected by change of temperature.

Flash ADC (or Parallel comparator ADC) :-

A flash ADC, also termed as parallel comparator ADC, finds application when very high speed is required. The ADC is called flash ADC, since it does the conversion very rapidly. Although a flash ADC is perhaps the simplest of converters, it is also the most expensive, since it uses a large no. of comparators.

figure shows the basic circuit of a flash type 3-bit A to D converter.



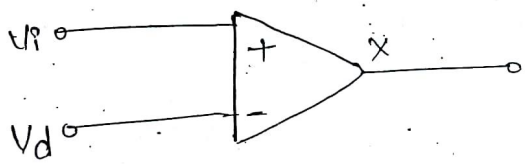
The circuit consists of a resistive divider network, 8 numbers of OpAmp comparators and a 8-line to 3-line priority encoder. The non inverting (+) i/p terminals of all opamps are connected to the analog i/p Vi and the inverting (-) i/p terminals are connected to various levels of the reference voltage VR produced by the resistive divider network, as shown in the figure.

The reference voltage V_R is equal to the full scale i/p signal voltage.

All resistors are of equal magnitude, the voltage levels at the nodes are equally devided between reference voltage V_R and the ground

The main purpose of building the circuit in the fashion shown in the figure is to compare the i/p analog circuit V_i with each of the node voltages.

The truth tables for the comparator and the ADC are given in figure



voltage i/p	Logic o/p X
$V_i > V_d$	$X = 1$
$V_i < V_d$	$X = 0$
$V_i = V_d$	previous value

i/p voltage V_i	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y
0 to 1/8 V_R	0	0	0	0	0	0	0	1	0	0	0
1/8 V_R to 1/4 V_R	0	0	0	0	0	0	1	1	0	0	1
1/4 V_R to 3/8 V_R	0	0	0	0	0	1	1	1	0	1	0
3/8 V_R to 1/2 V_R	0	0	0	0	1	1	1	1	0	1	1
1/2 V_R to 5/8 V_R	0	0	0	1	1	1	1	1	1	0	0
5/8 V_R to 3/4 V_R	0	0	1	1	1	1	1	1	1	0	1
3/4 V_R to 7/8 V_R	0	1	1	1	1	1	1	1	1	1	0
7/8 V_R to V_R	1	1	1	1	1	1	1	1	1	1	1

As studied earlier, the comparators give output 1 or 0 depending upon whether the i/p signal level is greater or less then the reference voltage level. A comparator whose o/p is a logical 1 remains ON, and a comparator whose o/p is a logical 0 remains OFF. The encoder converts the code resulting from the comparators into a binary code, and this is suitably displayed.

The number of comparators required for n-bit resolution $= 2^n - 1$

Quantization error $= \pm 1/2$ LSB

$f_{max} = \frac{1}{2\pi T_c \cdot 2^n}$, where f_{max} = maximum frequency for a sinusoidal i/p voltage to be digitized colthinan accuracy of $\pm 1/2$ LSB

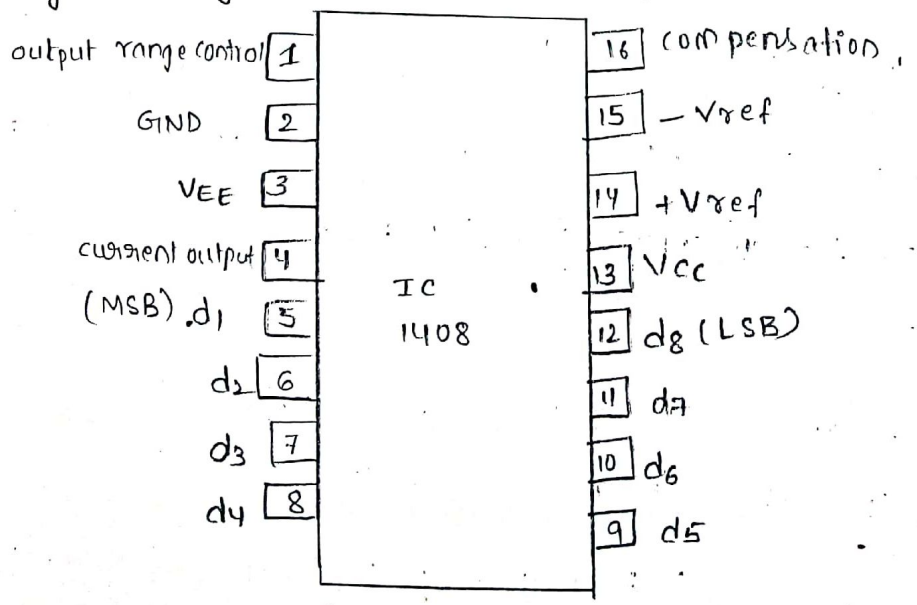
T_c = conversion time and

n = number of bits.

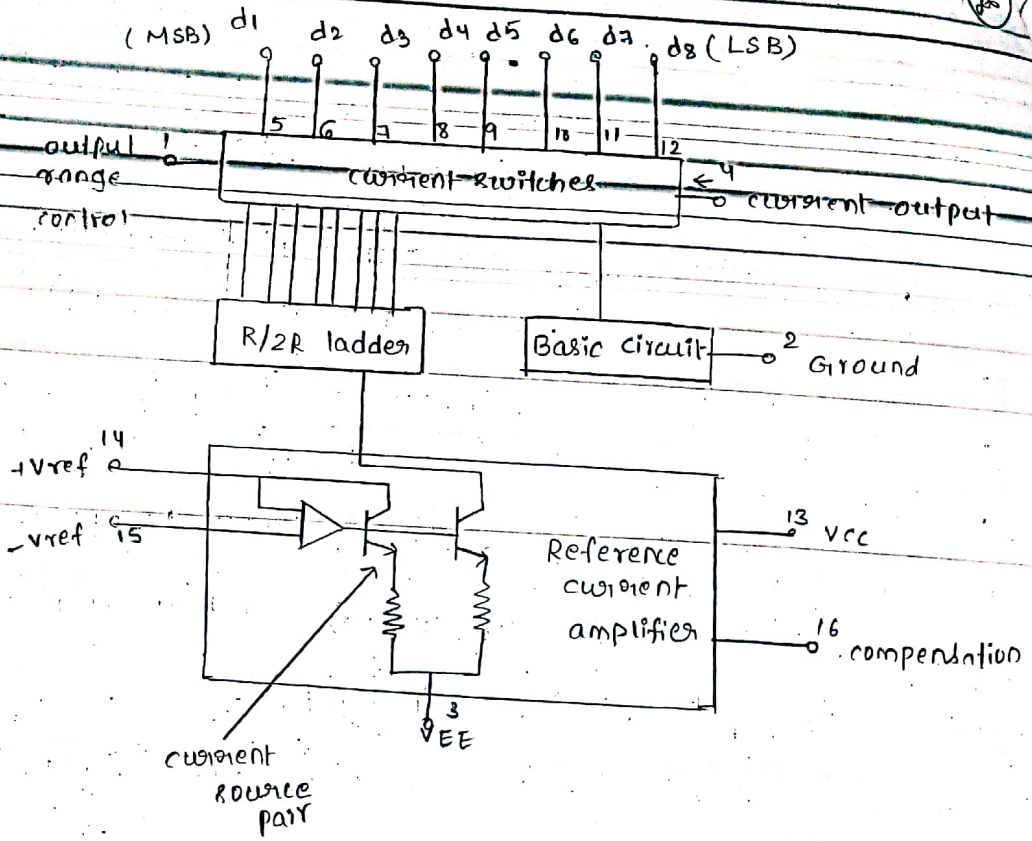
A monolithic DAC mainly consists of R-2R ladder, switches and the feedback resistor, all incorporated in a single chip. Such DAC's are available for 8 bit (or) 16 bit resolution.

The 8-bit DAC 1408 is one such typical monolithic IC, with a current output. The converter is a compatible with both TTL and cmos logic. It has a setting time of 300ns. There are 8 input data lines $d_1, d_2, \ldots d_8$. d_1 is the MSB and d_8 is the LSB. It requires two power supplies: $V_{CC} = +5V$, and $-V_{EE} = -5V$ and a reference current of 2mA for full scale input.

The pin diagram and block diagram of 8-bit DAC 1408 ar as given in fig.



pin diagram



Block diagram.

The reference voltage Vref and resistor R14 determine the total reference current source. Resistor R15 is equal to R14 so as to match the input impedance of the reference current amplifier.

A typical circuit of IC1408 DAC is given in fig.

The output current Io is given as

$$I_o = \frac{V_{ref}}{R_{14}} \left[\frac{d_1}{2^1} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \frac{d_4}{2^4} + \frac{d_5}{2^5} + \frac{d_6}{2^6} + \frac{d_7}{2^7} + \frac{d_8}{2^8} \right]$$

(or)

$$I_o = \frac{V_{ref}}{R_{14}} \sum_{i=1}^{8} d_i 2^{-i} \; ; \; d_i = 0 \text{ or } 1$$

D-A converter:- Digital to Ana

Errors:-

(31)

(27)

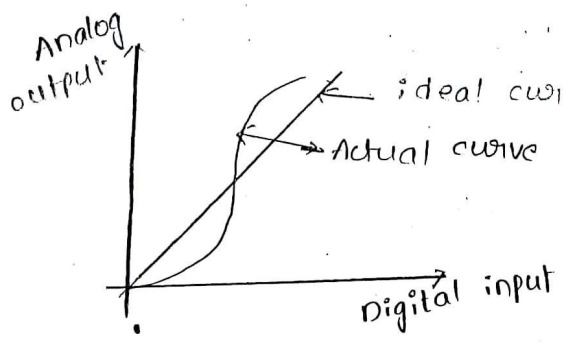
In relation to digital to analog converters, there are three types of errors.

i) Linearity error ii) offset error iii) Grain error.

These are discussed briefly.

i) Linearity error:- It was seen earlier that the transfer characte of a DAC (i.e graph of output voltage Vs input voltage) is practically a straight line passing through the origin. See the fig However in actual practice, the transfer curve may not be exac linear.

Linearity error may be defined as the difference between the actual output and the ideal output of DAC. This is made clear in fig.



linear error is caused mainly by errors in this current source resistor values.

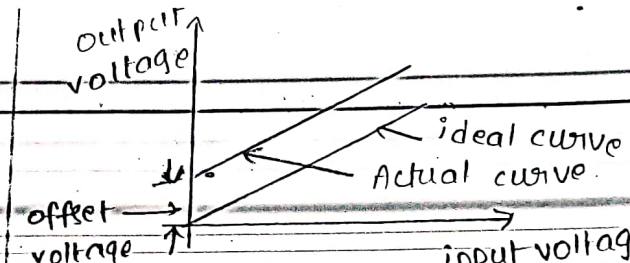
offset curve:-

Ideally when the input to the DAC is zero, the output must be zero. But in practical DAC, it is observed than ever for zero input, there is a small output voltage. this is due to the fact that the op amp. used in DAC circuit. has the offset voltage and leakage currents are present in the current switches

$V_o = -V_i$ (or) $V_o = V_i$

e both half cycles of the i/p signals conduction

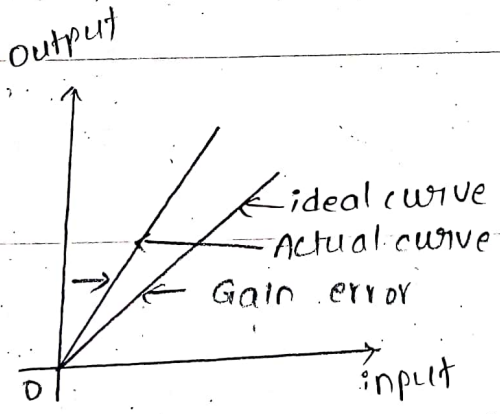
e a[illegible] o/p voltage $V_o = V_i$



offset error is defin[illegible] as the non-zero level of the output voltage, when the input is zero.

offset voltage is = OA from the fig.

iii) Gain error:-



Gain error is defined as the difference between the calculated gain and the actual gain, in relation to a current-to-voltage converter.

Gain error is caused by errors in the feed back resistor of the op amp.

Analog to

D-A conver

parameters & D to

Some

&

(i) Resolution (ii) [illegible]

(v) conversion time (vi) monotonocity

these are discused briefly.

Resolution :-

Resolution of DAC may be defined as the important number of different analog output values that DAC can provide.

for n- bit input word, the number of possible outputs $= 2^n$

$\therefore$ for n-bit DAC resolution $= 2^n$

Ex:

(i) for a 4-bit DAC, resolution $= 2^4 = 16$

(ii) for a 8-bit DAC, resolution $= 2^8 = 256$

Alternatively, resolution may be defined as the change in the output voltage of the DAC caused by a change of 1 LSB of the digital input.

for a n-bit DAC, resolution = $\frac{V_{OFS}}{2^n-1}$, where V_{OFS} is the full scale output voltage. (30)

Accuracy :-

ideally the output voltage of DAC should not differ from the expected output (or) at the worst, the difference should not exceed $\pm\frac{1}{2}$ of its LSB.

we have accuracy = $\frac{V_{OFS}}{(2^n-1)2}$, where V_{OFS} = full scale output voltage.

Let n = 8 and V_{OFS} = 5.1 V.

we have accuracy = $\frac{5.1}{(2^8-1)2}$ = 10 mv.

Stability :-

Changes of temperature, variations in power supply, and long usage affect the performance of a DAC. The device parameters like gain, linearity error, offset and monotonocity which are liable to change, must therefore be specified over the entire range of variations of power supply and temperature.

these parameters provide a measure of the stability of the DAC.

(iv) Setting time :

The setting time of DAC is defined as the time required for the output to settle to within $\pm \frac{1}{2}$ LSB of the final value, for a given digital input.

(v) Conversion time :

It may be defined as the time needed for the conversion of a digital input signal to its equivalent analog signal. It is affected by the response time of the switches and the amplifier output.

(vi) Monotonicity :-

A DAC is said to have good monotonicity, if it does not miss any step backward, when stepped through its entire range by a counter.

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UNIT-6

D/A AND A/D CONVERTERS

Introduction :-

→ Most of the information carrying signal such as vtg, ct, temp, pressure, force, charge etc.. are available in analog quantities. are measured using transducer (or) sensor.

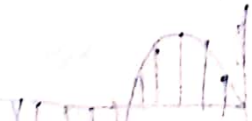
→ Generally, the transducer or sensor o/p is an analog form

→ If the process (transmit (or) store) these analog signals may getting errors so convert analog signal in digital signals and then process.

→ If we use digital signal, it reduces noise and provide better accuracy.

→ The analog signal has infinite values but the digital signal only two values.

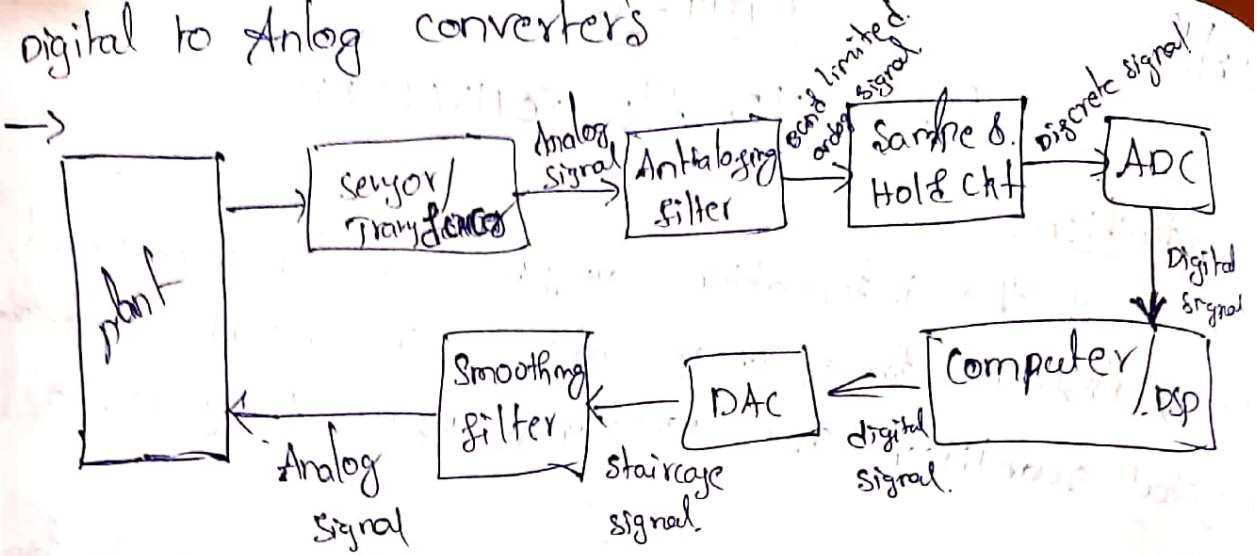
→ Digital to Analog converter is used for converting digital data into analog data.



→ for example is a computer is used as a ~~computer~~ controller

→ A computer always generates the control signal and digital form, the system to be controlled requires the Analog signal, at this case it requires

digital to Analog converter's



Sensor (or) Transducer :-

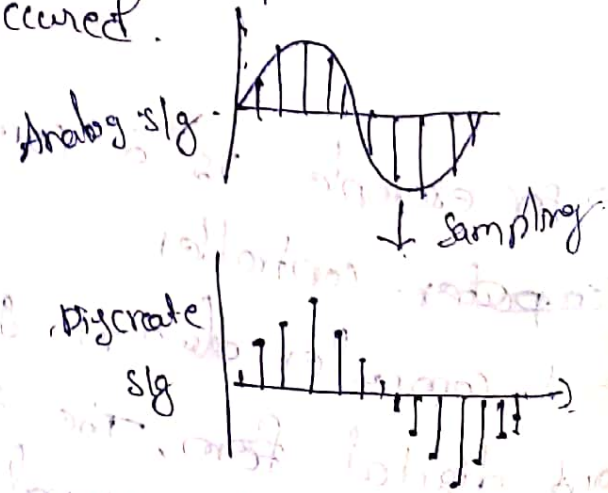
→ It measures variations in physical quantity (Temp, pressure, humidity etc---)

Antialoging filter :-

It is a low pass filter and it eliminates high frequency components and allows only low frequency components.

- Sample & Hold ckt :-

It samples the analog signal at regular intervals and hold's the last sampled value until the next sample occured.



ADC :- It converts sampled Analog signal into it's equal and digital signal.

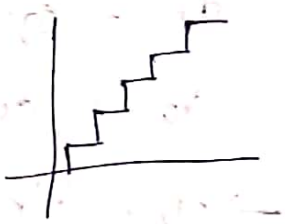
Computer (or) digital signal processor :-

The output of ADC is digcreate, here control algorithm is loaded, this algorithm is loaded, measured value is a set value.

→ If this value of measured is more (or) less than the set value then it generates a control signal in the form of digital

DAC :-

It converts Digital signal into staircase signal



Smoothing filter :-

It eliminates quantization noice and produces true analog signals.

⇒ The above example is used in following.

i) digital audio recording and play back.

ii) cying and ~~radio~~ video systhesy

iii) Direct digital control.

iv) Data Acquisition.

v) Digital signal processing

vi, Micro processor based instrumentation.

vii, pulse code modulation & transmission.

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Basic DAC Techniques :-

$$V_0 = K V_{FS}\left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right) \rightarrow (1)$$

where,

K = scaling factor = 1

generally designed to unity

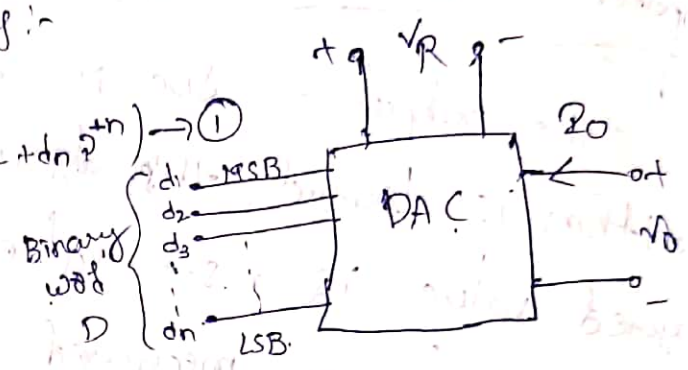


Fig :- schematic of DAC

V_{FS} = full scale op vtg

d_1 = most significant bit

d_n = least significant bit

V_0 = output vtg

→ The i/p binary data word is converted into Anlog signal with they help of reference vtg

→ The o/p of the DAC can be either current (or) vtg

→ The DAC Techniques are

1. weighted resistor DAC
2. R-2R ladder DAC
3. Inverted R-2R ladder DAC
4. multiplaying DAC.

~~1. weighted resistor DAC~~

(1). weighted resistor DAC :-

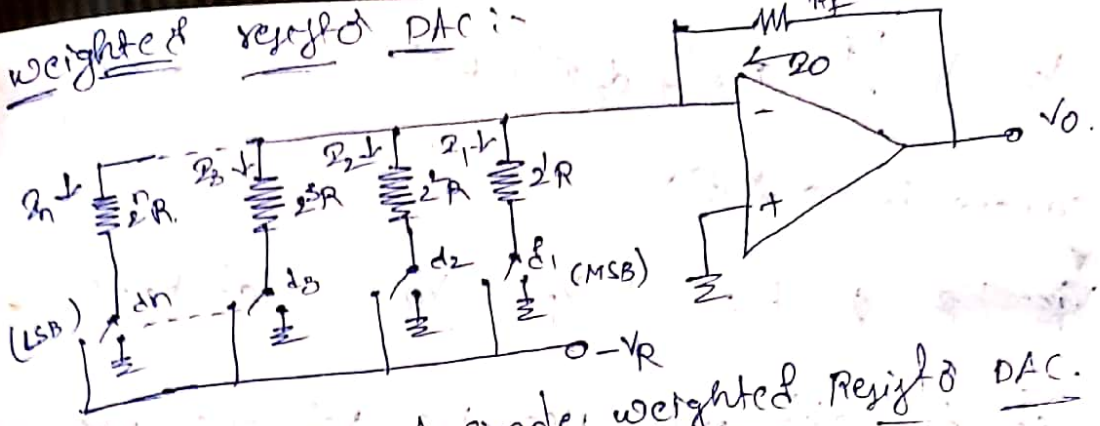


Fig: A simple weighted Resistor DAC.

→ The ckt uses Summing Amplifier and weighted resistor network.

→ It has n-electronic switches controlled by i/p binary data

→ All switches are SPDT type switches (single pole double throw)

→ The binary data to a particular switch is one, it connects the resistor to reference vtg

→ The binary i/p to a particular switch is zero, it connects resistor to ground connection.

→ Assume op-Amp is ground position Apply KCL at node (A).

$$I_0 = I_1 + I_2 + I_3 + \cdots + I_n$$

$$I_0 = \frac{V_R}{2^1 R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \cdots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n} \right]$$

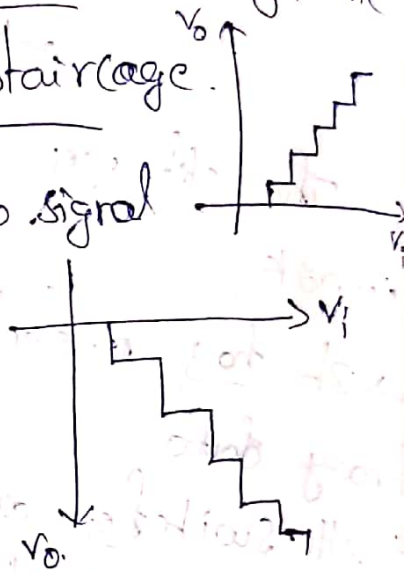
$V_0 = -I_0 R_f$

$$V_0 = V_R \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right] \rightarrow (2)$$

Compare to (1) & (2).

$k = 1$; $V_{FS} = V_R$ let $R_f = R$

→ let, the ckt uses negative reference vtg, the Analog o/p vtg is a 'tve' staircase.



→ for 'tve' ref vtg the analog o/p signal is a '-ve' staircase.

→ The op-Amp connected in inverting mode, it can also be connected in Non-inverting mode.

→ The op-Amp simply working as a cf to vtg converter.

→ The polarity of reference vtg is choosen according to the type of switch used.

→ The accuracy and stability of DAC depends on accuracy of the resistors and the tracking of each other with temp.

Eg:- 3 bit weighted resist DAC.

let $R_f = R$.

$$(2) \Rightarrow V_0 = V_R\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right)$$

(d_1: MSB, d_3: LSB)

D = 0 0 0 ⟹ $V_0 = 0$

0 0 1 ⟹ $V_0 = V_R(0\times2^{-1} + 0\times2^{-2} + 1\times2^{-3}) = \frac{V_R}{8}$

0 1 0 ⟹ $V_0 = V_R(0\times2^{-1} + 1\times2^{-2} + 0\times2^{-3}) = \frac{V_R}{4} = \frac{2V_R}{8}$

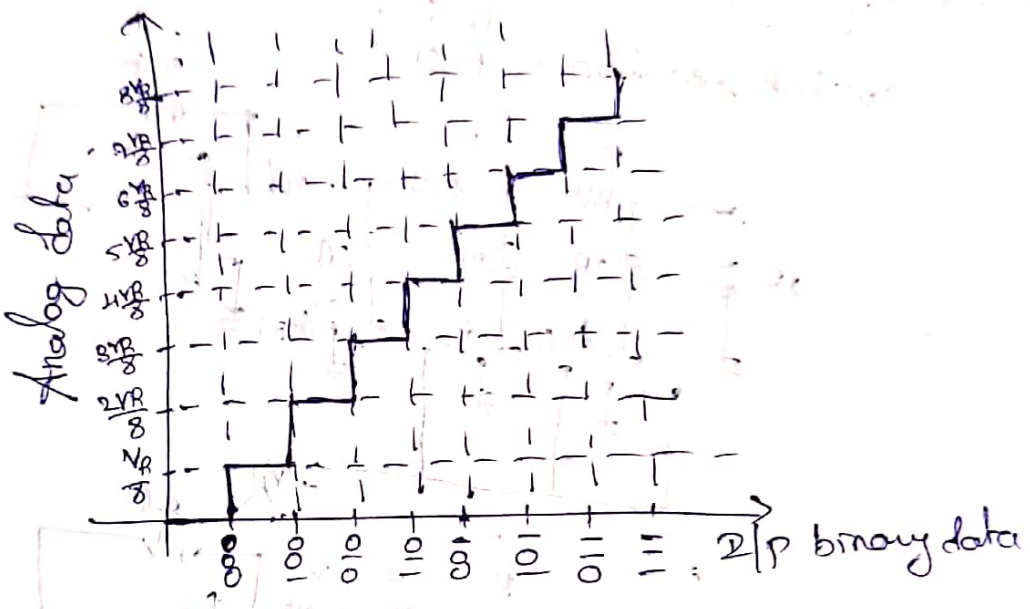
0 1 1 ⟹ $V_0 = V_R(0\times2^{-1} + 1\times2^{-2} + 1\times2^{-3}) = \frac{3V_R}{8}$

1 0 0 ⟹ $V_0 = V_R(1\times2^{-1} + 0\times2^{-2} + 0\times2^{-3}) = \frac{V_R}{2} = \frac{4V_R}{8}$

1 0 1 ⟹ $V_0 = V_R(1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3}) = \frac{5V_R}{8}$

1 1 0 ⟹ $V_0 = V_R(1\times2^{-1} + 1\times2^{-2} + 0\times2^{-3}) = \frac{6V_R}{8}$

1 1 1 ⟹ $V_0 = V_R(1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3}) = \frac{7V_R}{8}$



Ex 8/19

Drawback in weighted Resistor DAC :-

wide range resistor value required for better resolution i/p binary value as to be increased, it increases a range of resistor.

Eg:- 3 bit → 2^0R, 2^1R, 2^2R

8 bit → 2^0R, 2^1R ---2^7R

8 different reg value.

for R = 2.5 kΩ

Smallest resistor = 2.5 kΩ

Largest resistor = $2^7 \times 2.5k = 5.12 M\Omega$

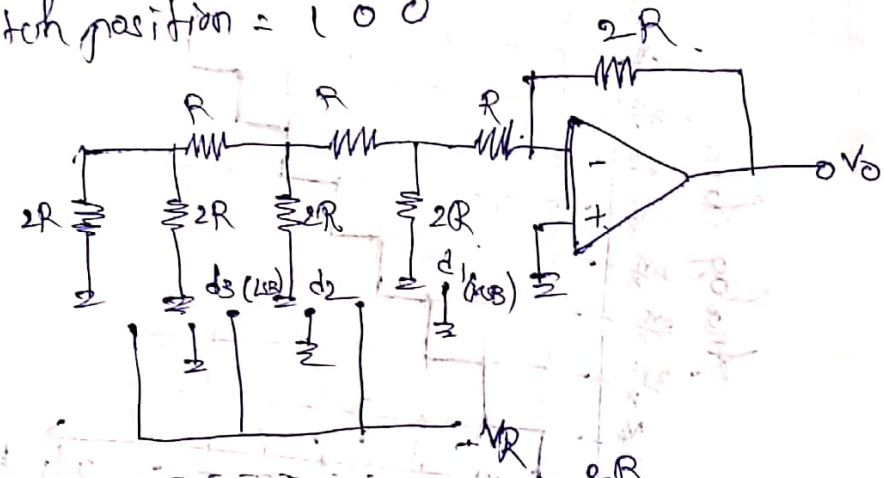
R-2R ladder DAC is wide range of resistor requiring weighted resistor are this can be avoided by using R-2R ladder DAC.

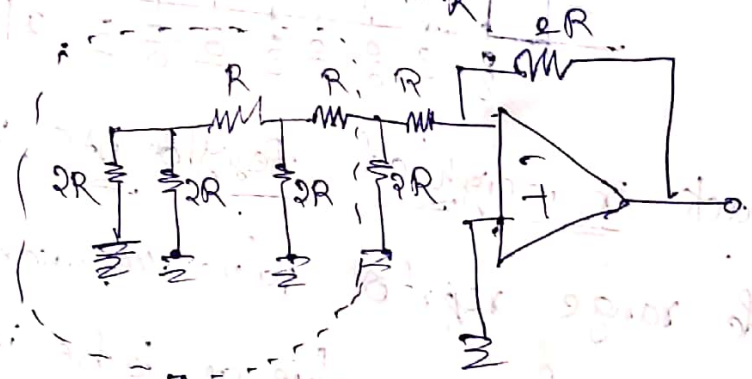
→ The ckt requires only two resistor values so, it is well suited for integrated ckt realization

→ simplicity, Consider 3 bit data, switch position

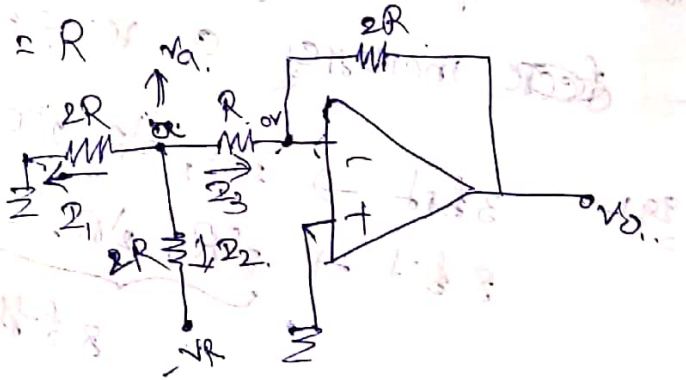
$d_1\ d_2\ d_3$

switch position = 1 0 0





$\frac{2R \times 2R}{4R} = R$



$$I_1 = \frac{V_a - 0}{2R} \quad I_2 = \frac{V_a + V_R}{2R} \quad I_3 = \frac{V_a - 0}{R}$$

Apply KCL at node A, $I_1 + I_2 + I_3 = 0$

$$\frac{V_a}{2R} + \frac{V_a + V_R}{2R} + \frac{V_a}{R} = 0$$

$$\frac{V_a + V_a + V_R + 2V_O}{2R} = 0$$

$$2V_a + V_R + 2V_O = 0$$

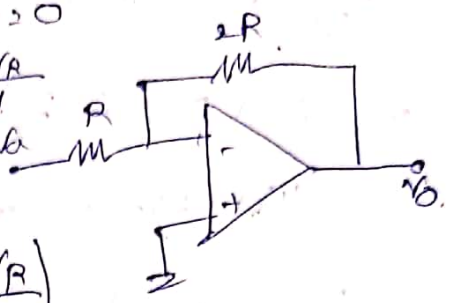
$$4V_a + V_R = 0$$

$$V_a = \frac{-V_R}{4}$$

$$V_O = \frac{-2R}{R} V_a$$

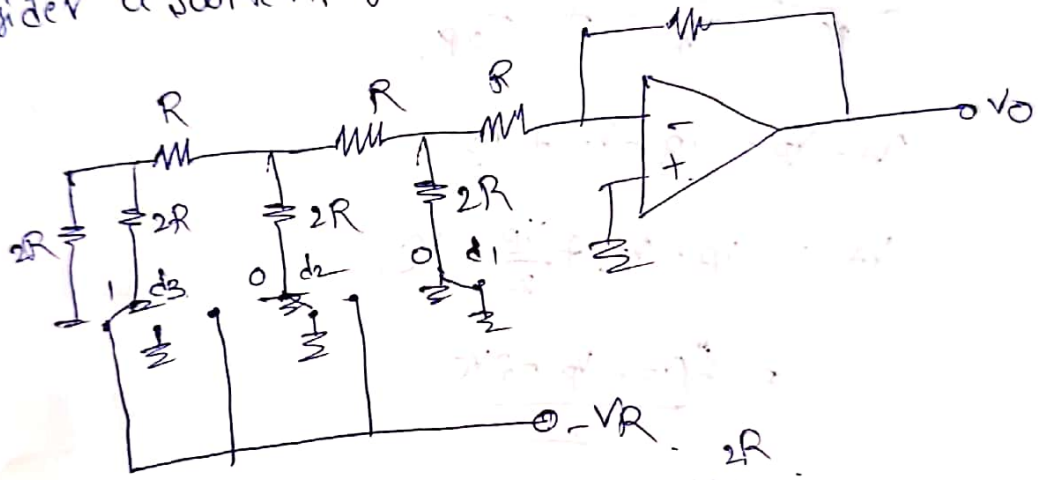
$$V_O = \frac{-2R}{R}\left(\frac{-V_R}{4}\right)$$

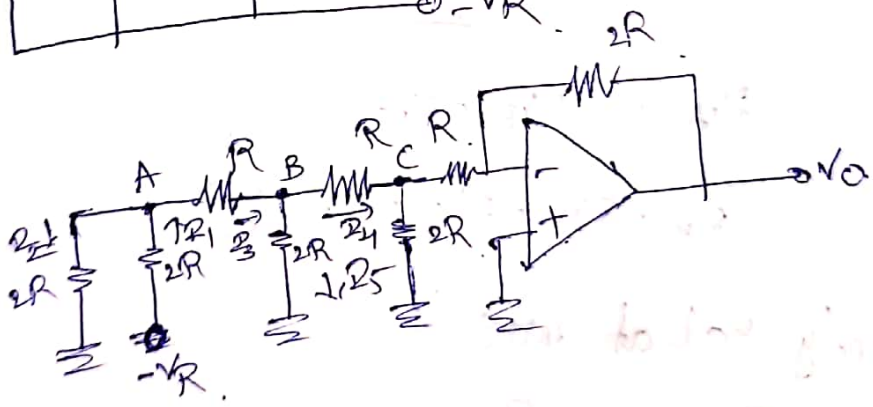
$$\boxed{V_O = \frac{V_R}{2}}$$



$d_1 d_2 d_3$.

Consider a switch position 001





Apply KCL at node A.

$$I_1 = I_2 + I_3$$

$$\frac{-V_R - V_A}{2R} = \frac{V_A - 0}{2R} + \frac{V_A - V_B}{R}$$

$$\frac{-V_R - V_A}{2R} = \frac{V_A}{2R} + \frac{V_A - V_B}{R}$$

$\Rightarrow \frac{-V_R}{2} - \frac{V_A}{2} = \frac{V_A}{2} + V_A - V_B.$

$-\frac{V_R}{2} = \frac{V_A}{2} + \frac{V_A}{2} + V_A - V_B.$

$\Rightarrow 2V_A - V_B = -\frac{V_R}{2}$

$4V_A - 2V_B = -V_R \rightarrow (1)$

→ Apply KCL at node B.

$I_3 = I_4 + I_5$

$\frac{V_A - V_B}{R} = \frac{V_B - V_C}{R} + \frac{V_B - 0}{2R}$

$V_A - V_B = V_B - V_C + \frac{V_B}{2}$

$V_A = V_B + V_B + \frac{V_B}{2} - V_C$

$= \frac{2V_B + V_B - 2V_C}{2}$

$2V_A = 5V_B - 2V_C$

$2V_A - 5V_B + 2V_C = 0 \rightarrow (2)$

Apply KCL at node 'C'

$I_4 = I_5 + I_6$

$\frac{V_B - V_C}{R} = \frac{V_C}{2R} + \frac{V_C}{R}$

$V_B - V_C = \frac{V_C + 2V_C}{2}$

$2V_B - 2V_C = 3V_C$

$\Rightarrow 2V_B - 5V_C = 0 \rightarrow (3)$

solve eq^n ①, ② & ③.

$4V_A - 2V_B = -\frac{V_R}{8}$ → ①

$2V_A - 5V_B + 2V_C = 0$ → ②

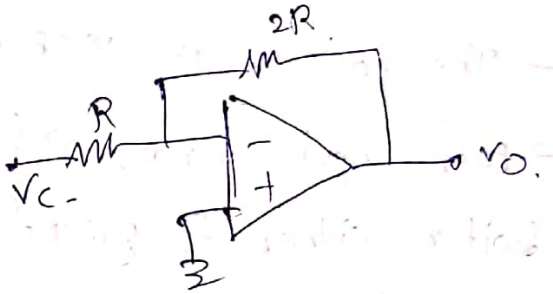
$2V_B - 5V_C = 0$ → ③

$V_A = -\frac{21}{64} V_R$; $V_B = \frac{-10}{64} V_R$; $V_C = \frac{-1}{16} V_R$.

∴ The.

$V_0 = \frac{-2R}{R} V_C$

$= -2\left(\frac{-1}{16} V_R\right)$



$$V_0 = \frac{V_R}{8}$$

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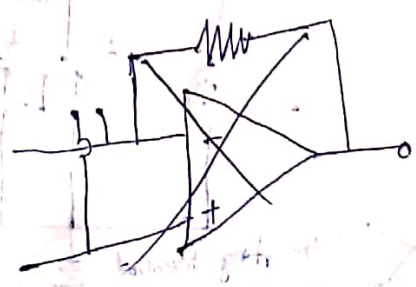
Drawback in weighted Resistor DAC & R-2R ladder DAC

→ The ct flowing in the resistor changes as the i/p data changes.

→ More power dissipation causes heating which intern creates non-linearity in DAC.

→ The above two problems can be avoided completely in inverter R-2R ladder DAC.

* Inverted R-2R ladder DAC :-



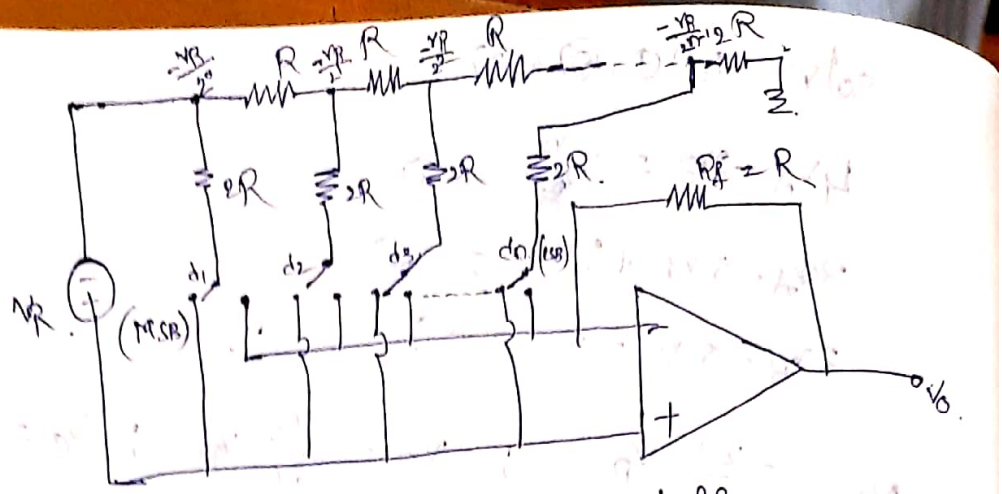


Fig: Inverted R-2R ladder DAC.

→ The position of MSB & LSB are interchanged.

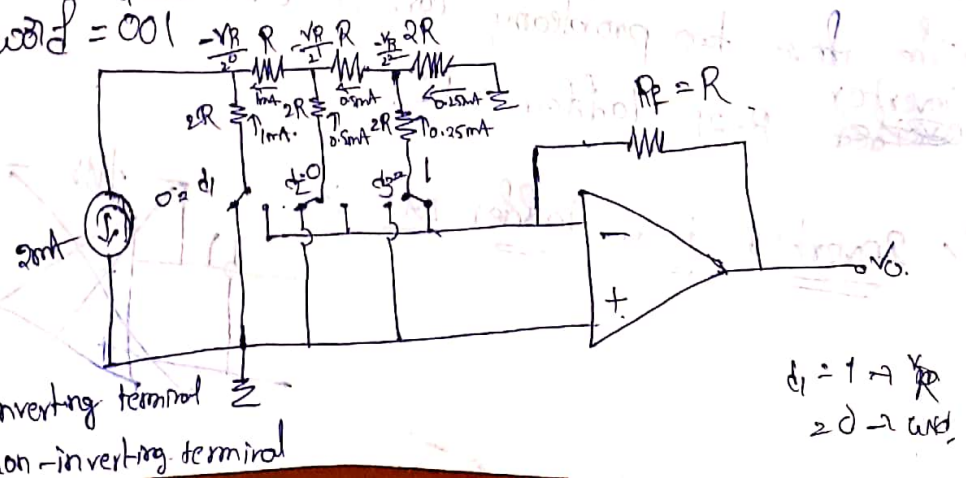
→ Each input binary word connects the corresponding switch either to ground (or) the inverting i/p terminal of operational Amplifier

→ It is also a virtual ground

→ since, both the terminals of switches are at a long protectional, ct through the resistor a constant and independent of the switch position.

→ The ckt has one important property then the ct divides equally at each of the nodes because the equivalent resistance to the right (or) left of any node is exactly ~~to~~ 2R

→ consider 3-bit inverted R-2R ladder DAC with i/p binary word = 001 ($d_1 d_2 d_3$)



d_i → 1 → Inverting terminal
0 → Non-inverting terminal

$d_1 = 1 \rightarrow V_R$
$= 0 \rightarrow$ GND

→ The ckt is independent of input binary word, These ckt's remain constant in each branch of the ladder

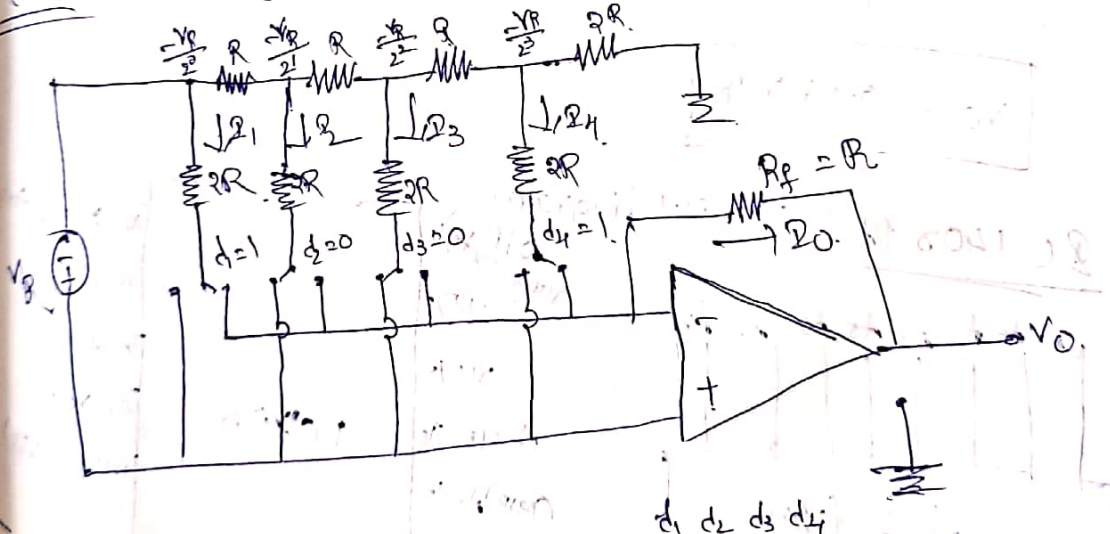
→ since, constant ckt implies constant vtg's, they ladder node vtg's remaine constant at $\frac{-V_R}{2^0}, \frac{-V_R}{2^1}, \frac{-V_R}{2^2}$ - - -

→ The ckt works are the principle of summing currents and it also set to operate in ct mode

Advantage :-

The ladder node vtg's remaine constant even with change in input binary word.

4 bit Inverted R-2R ladder DAC :-



Consider I/p binary word = 1001

$$I_1 = \frac{-V_R - 0}{2R} = \frac{-V_R}{2R}$$

$$I_2 = \frac{-V_R/2 - 0}{2R} = \frac{-V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{-V_R/4 - 0}{2R} = \frac{-V_R}{8R} = \frac{I_1}{4}$$

$$I_4 = \frac{-V_R/8 - 0}{2R} = \frac{-V_R}{16R} = \frac{I_1}{8}$$

$$I_0 = I_1 + I_2 + I_3 + I_4$$

o/p vtg $V_0 = -I_0 R_f$.

$$V_0 = -R_f \left[d_1 \frac{V_R}{2R} - \frac{V_R}{4R} d_2 - \frac{V_R}{8R} d_3 - \frac{V_R d_4}{16R} \right]$$

$$= \frac{R_f}{R} V_R \left[2^{-1} d_1 + 2^{-2} d_2 + 2^{-3} d_3 + 2^{-4} d_4 \right]$$

here $d_1 d_2 d_3 d_4 = 1001$

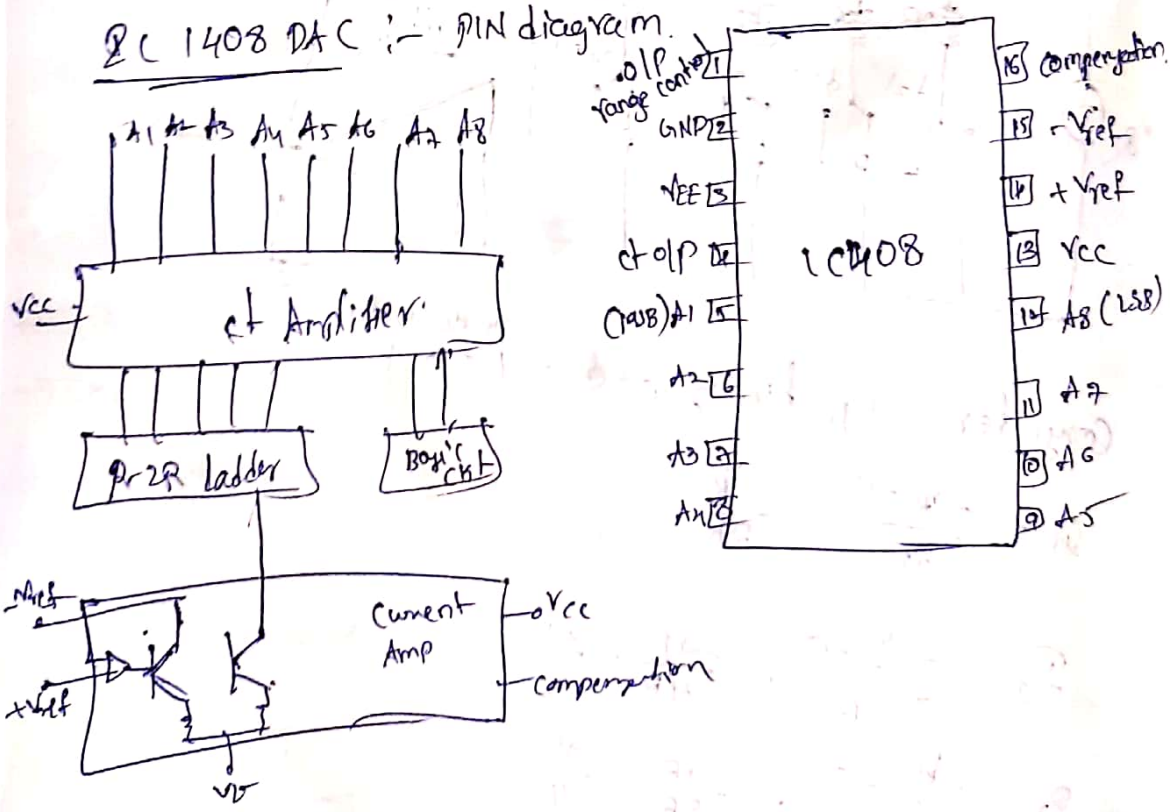
$$V_0 = \frac{R_f}{R} V_R \left[2^{-1} \cdot 1 + 0 + 0 + 2^{-4} \cdot 1 \right]$$

$R_f = R$

$$V_0 = \frac{R}{R} V_R \left[0.5625 \right]$$

$$\boxed{V_0 = 0.5625\, V_R}$$

IC 1408 DAC :- PIN diagram.



6/9/19 A-D converters :-

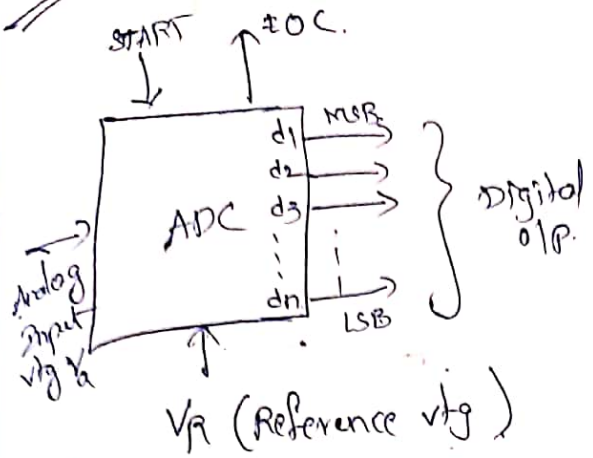


Fig :- Functional Block diagram of ADC.

→ It accepts analog i/p vtg 'Va' and produces o/p binary word $d_1, d_2, d_3 \dots d_n$

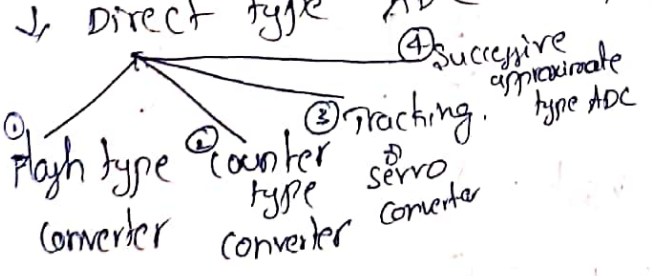
→ An ADC usually has two additional control signals

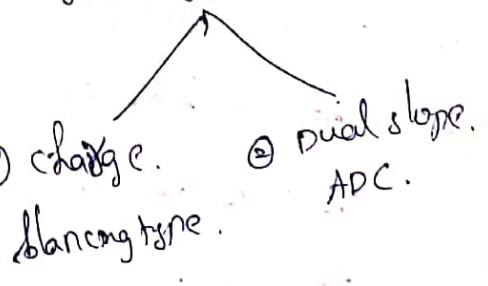
1, START → It tells when to start the conversion

2, EOC → (end of conversion) :- it announces when the conversion complete.

ADC are classified into two groups according to their conversion techniques

1, Direct type ADC 2, Integrating type ADC.





① Direct type ADC :-

② Flash type converter :-

④ Flash comparator type ADC :-

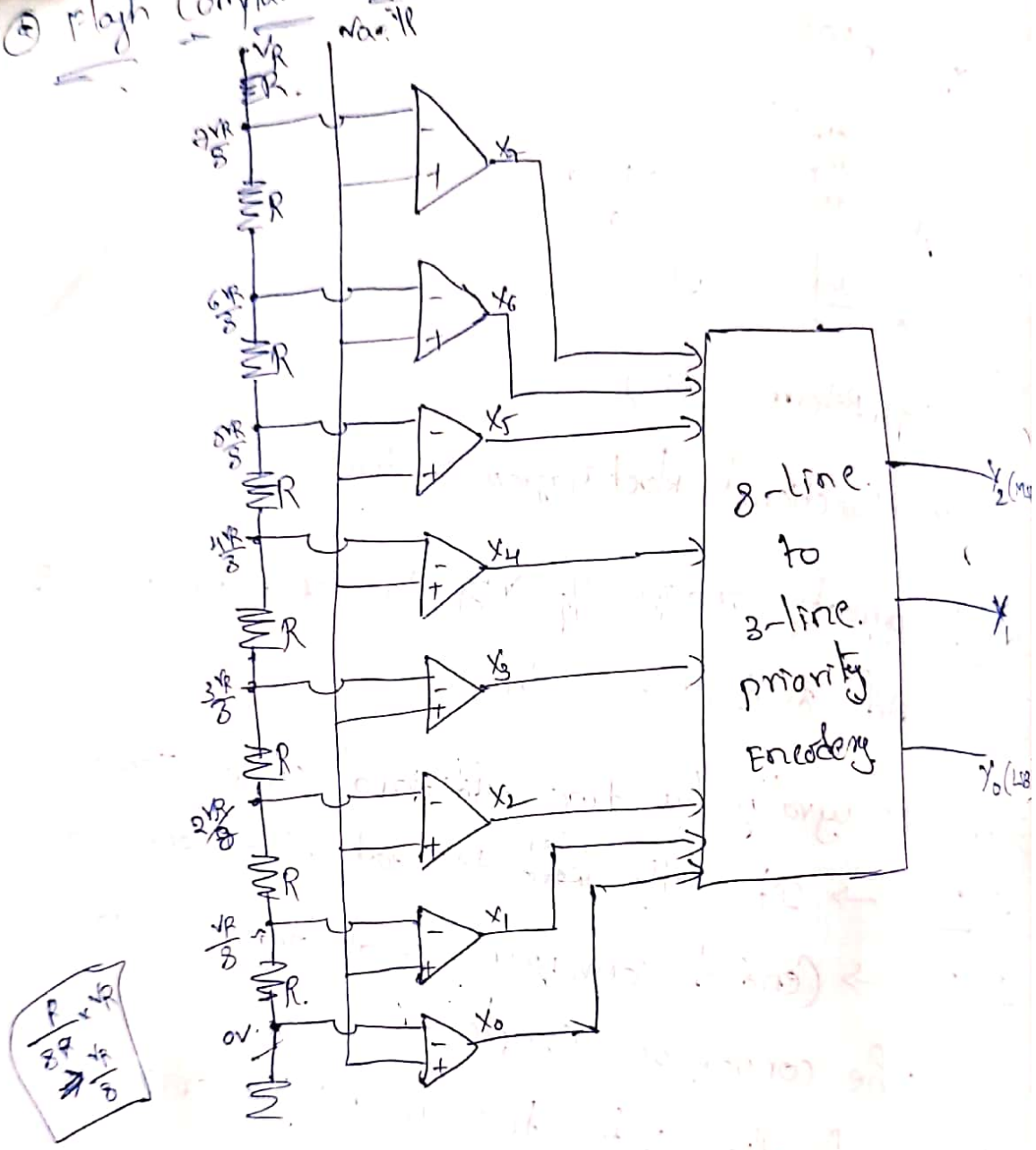
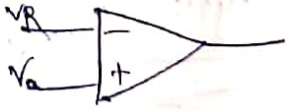


Fig:- Basic ckt of Flash type ADC.

→ It is a simplest technique, It is a fastest and most expensive technique



$V_a > V_R \Rightarrow V_0 = +V_{sat} = 1$

$V_a < V_R \Rightarrow V_0 = -V_{sat} = 0$

$V_a = V_R \Rightarrow V_0 =$ It maintance the previous parameter

Truth table :-

Input voltage	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

→ A small amount of hysteresis is built in comparator to reserved any problems that may occur both i/p's are equal values

Advantages :-

→ High speed as conversion takes place simultaneously either than sequentially

→ Fixed conversion time is 100ns (avg)

→ Conversion time is critical only the speed of the comparator and the priority encoder

→ By using, advanced micro devices AMD 686A comparator and 74147 priority encoder, the conversion delay of 20nsec can be obtained

Disadvantages :-

→ No. of comparators required almost doubles for each adder bit

for example : 2-bit ADC required 4 comparators

3 " " 8 "

4 " " 16 "

n " " 2^n "

② Counter type ADC :-

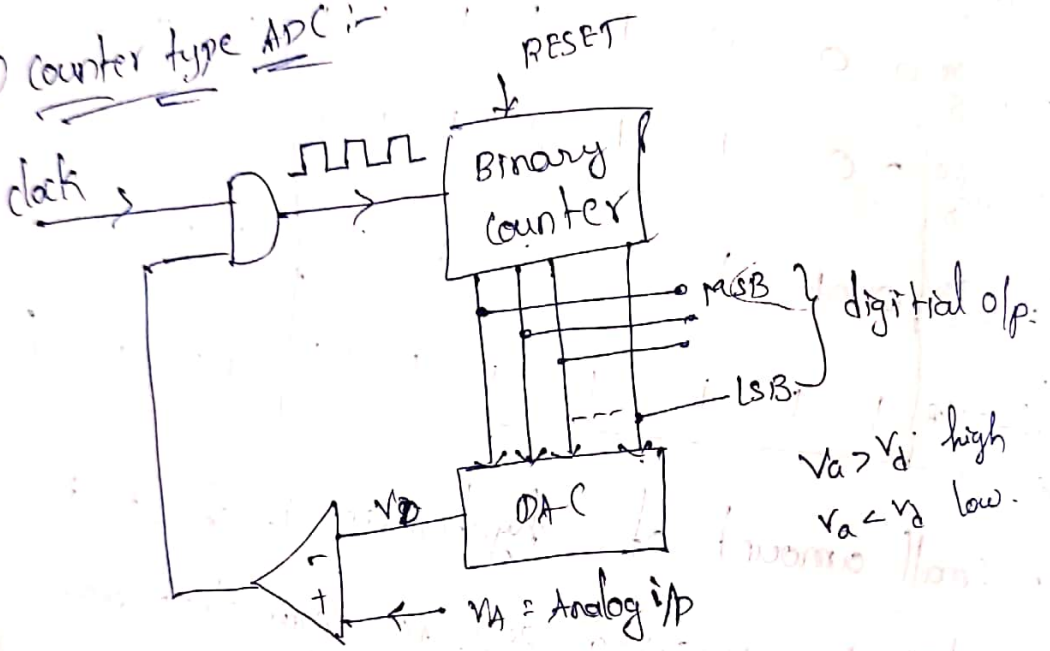


Fig :- counter type ADC

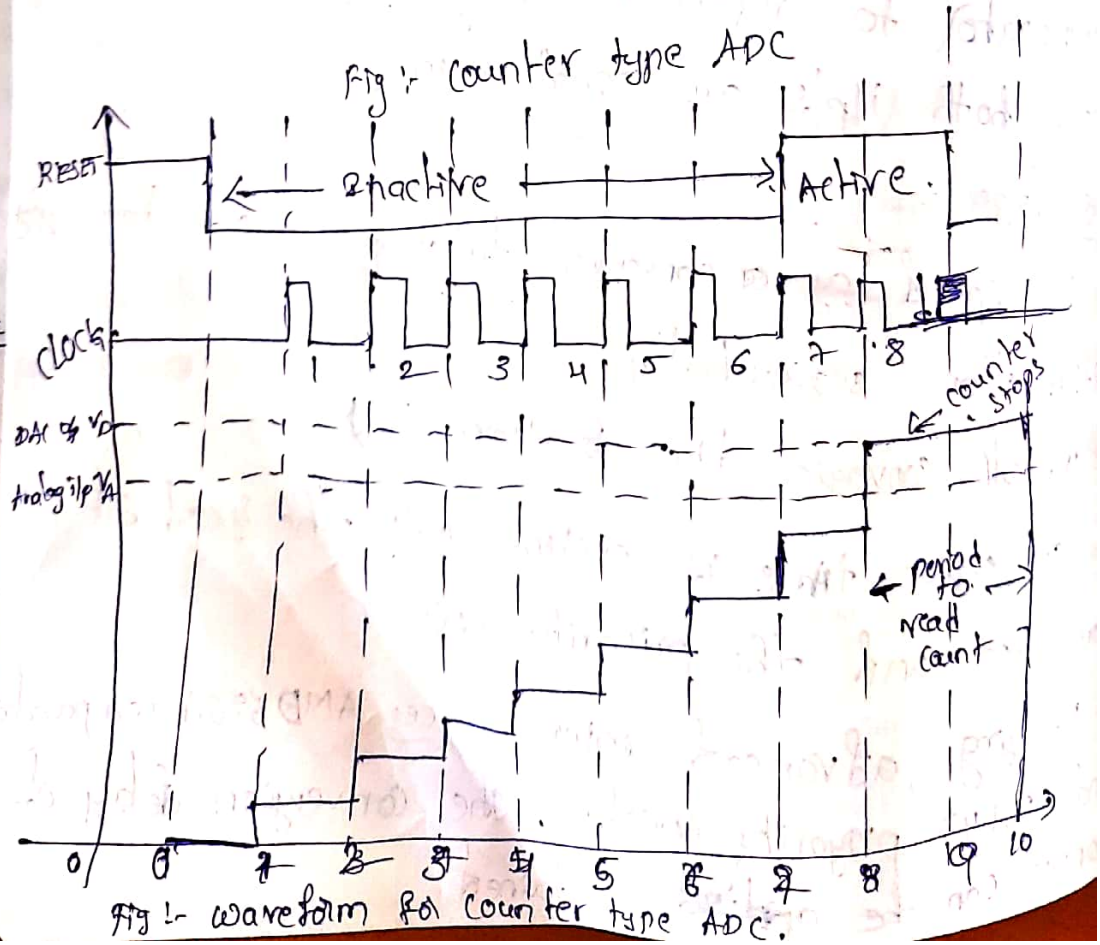
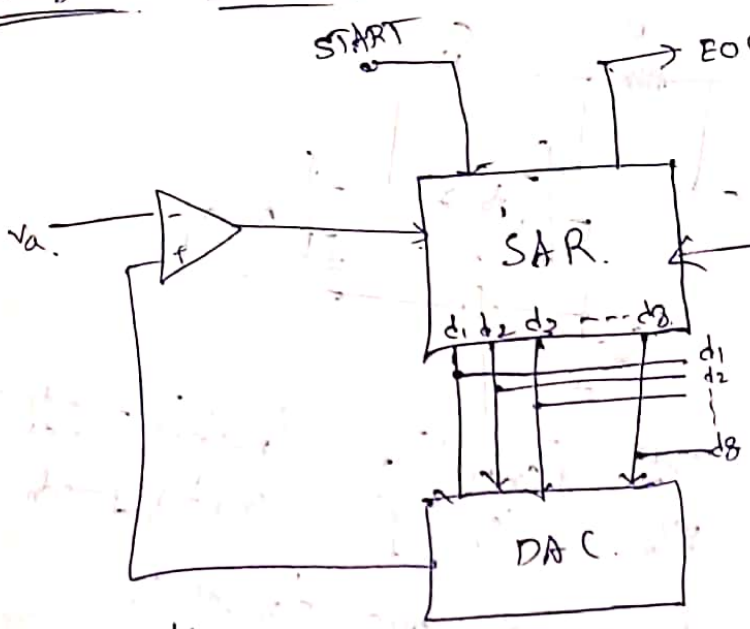


Fig :- waveform for counter type ADC.

Drawbacks:

1. It is necessary to enough time for DAC comparator
2. conversion time is not constant.
3. High voltage → convert time. Increase.

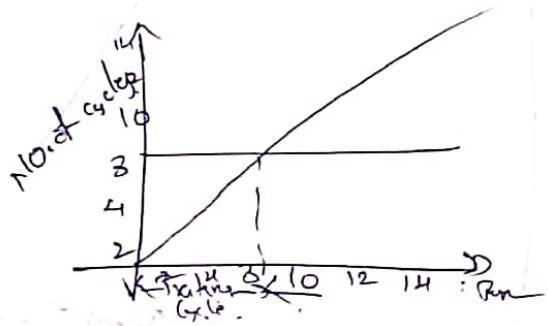
(3) Successive Approximation com :-



Analog.

Va > DAC ⇒ low

Va < DAC ⇒ high.



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Integrating type ADC's :-

Integrating type ADC do not require sample & hold ckt at the input.

Dual slop ADC :-

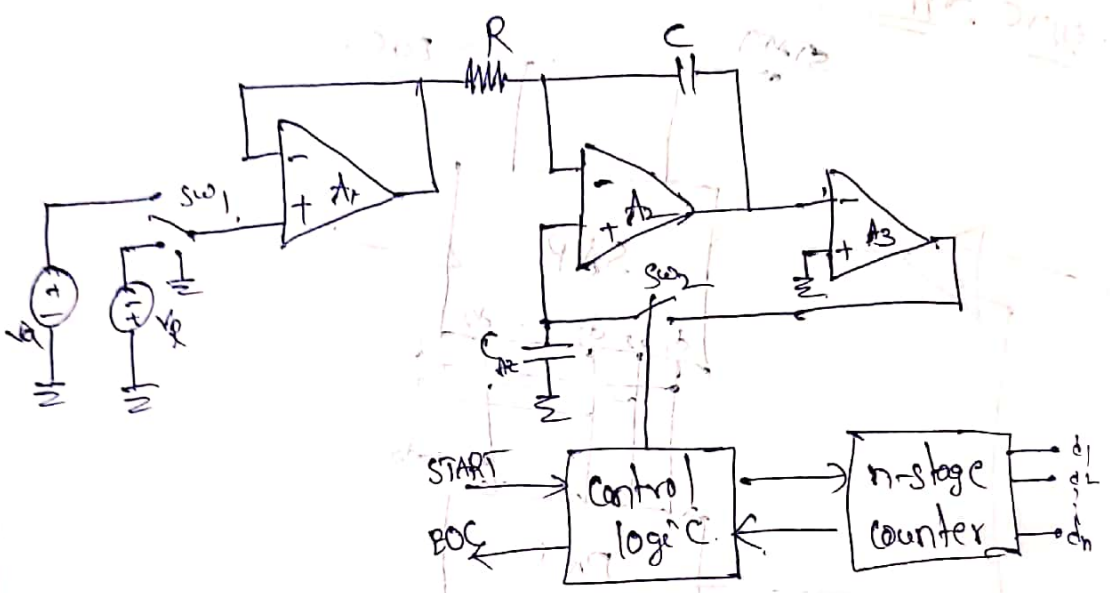

Fig: Functional diagram of dual slop ADC.

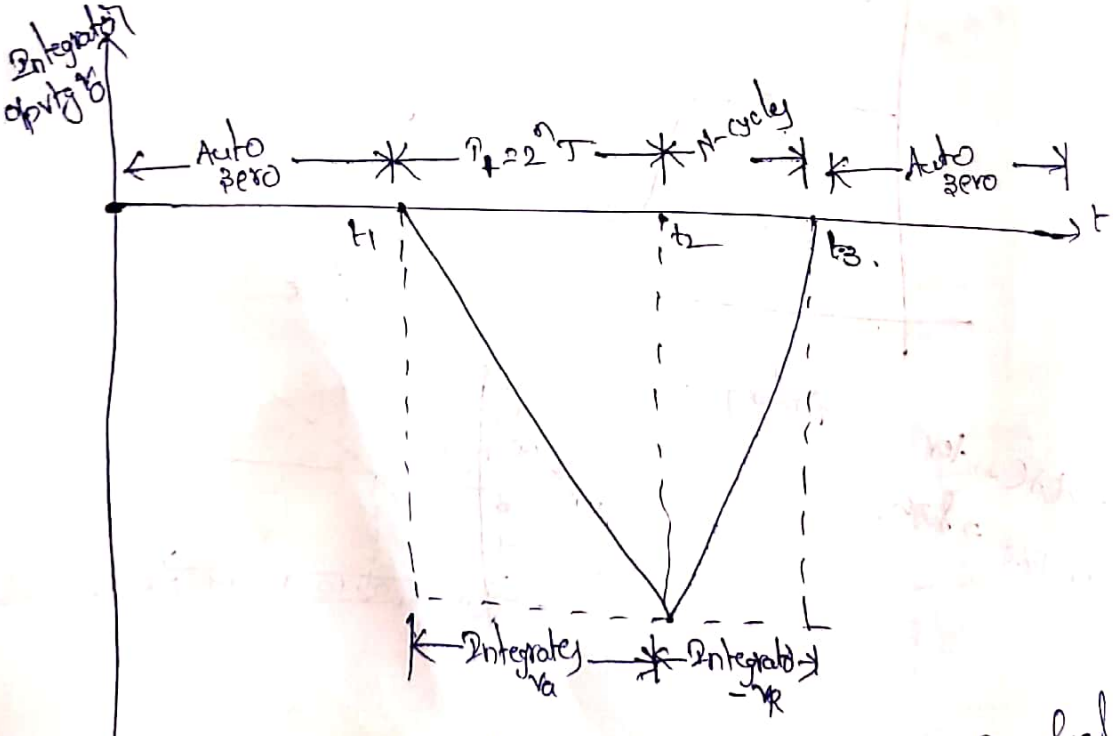

Fig (2): Integrator output waveform for dual slope ADC.

A_1 → a voltage follower (or) at high resistance buffer

A_2 → Integrator.

A_3 → Comparator

C_0 → Capacitor is used for compensating purpose that means it compensating's A_1, A_2 & A_3.

T_1 → time required for the integrator to Analog

T → " " to integrate the analog

operation :-

→ Before the START command.

- sw_1 → ground
- sw_2 → closed

→ Input offset vtg present in integrator

→ After applying the START command

- sw_1 → V_a
- sw_2 → C.L

→ RESET = 0

- sw_1 → $-V_R$.

N-cycle.