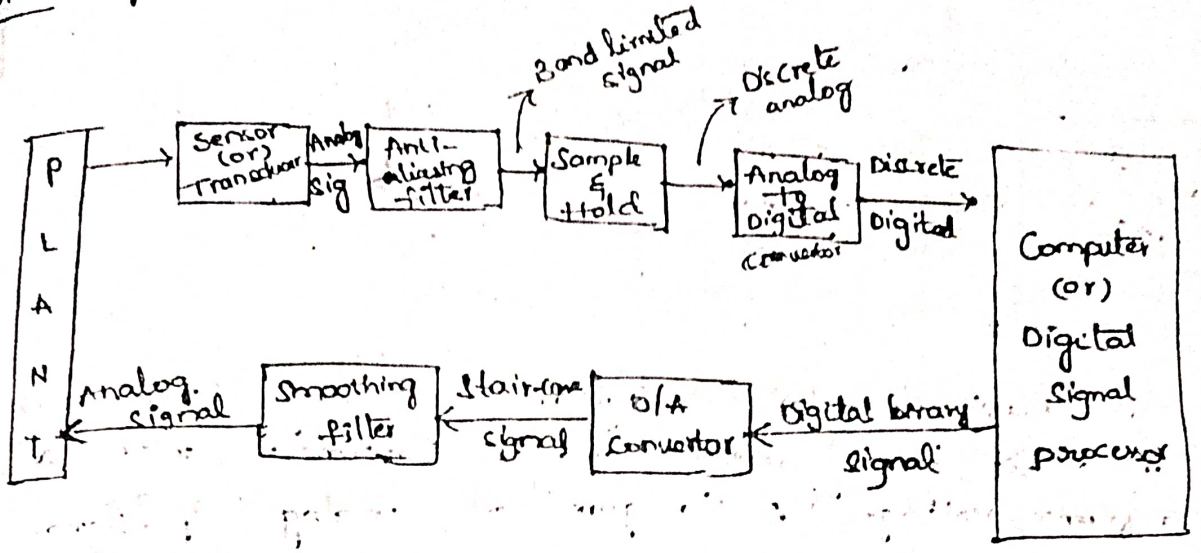
UNIT-6

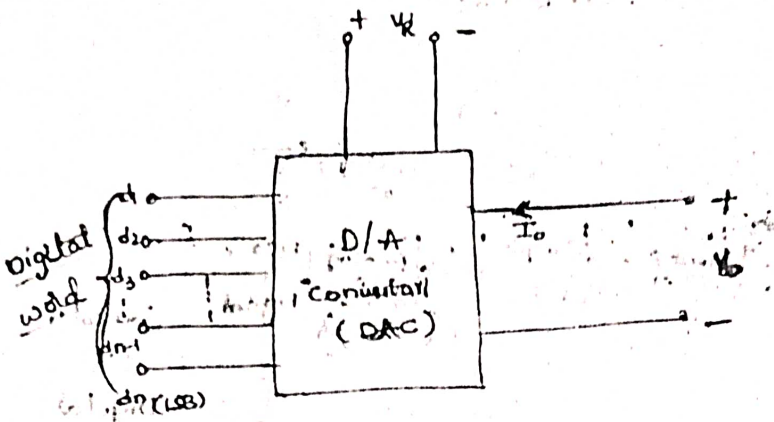
D/A & A/D Convertors

Block diagrams :-



From the Block diagram it uses the physical quantities like voltage, current, temperature, pressure and time etc which is applied as a i/p reference signal for the sensor (or) transducer which senses the particular i/p signal and it will produces the analog signal. This analog signal is applied to the anti-aliasing filter which reduces aliasing effect i.e., the overlapping of many signals and which gives the band limited signal only and it can be sampled and sometimes it is in hold state then the discrete analog signal is produced. This discrete analog signal is applied to analog to digital convertor which gives the o/p of discrete digital response. This response is applied to a mini computer (or) DSP which accepts only the binary i/p signal and that digital info applied to the D/A convertor which gives the stair case response signal this signal is applied to the smoothing filter which reduces unwanted noise then the o/p is analog signal.

Basics of DAC Techniques (Digital to Analog Convertor) :



The basic i/p for a digital to analog convertor is an n-bit binary word and is combined with a reference voltage V_R to give an analog o/p signal. The o/p of DAC may be voltage or current the D/A convertor is mathematically expressed as

$$V_o = k\, V_{FS} \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n} \right] \quad \text{---} (1)$$

where k is the scaling factor always adjusted to unity i.e. k = 1, V_{FS} is full scale voltage,

$d_1, d_2 \ldots d_n$ = digital binary word.

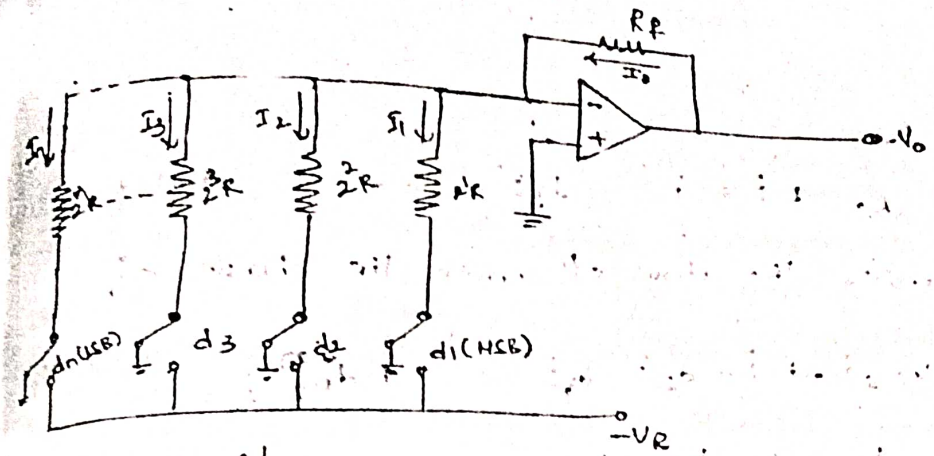
d_1 = most significant bit (MSB) with weightage of $\frac{V_{FS}}{2}$

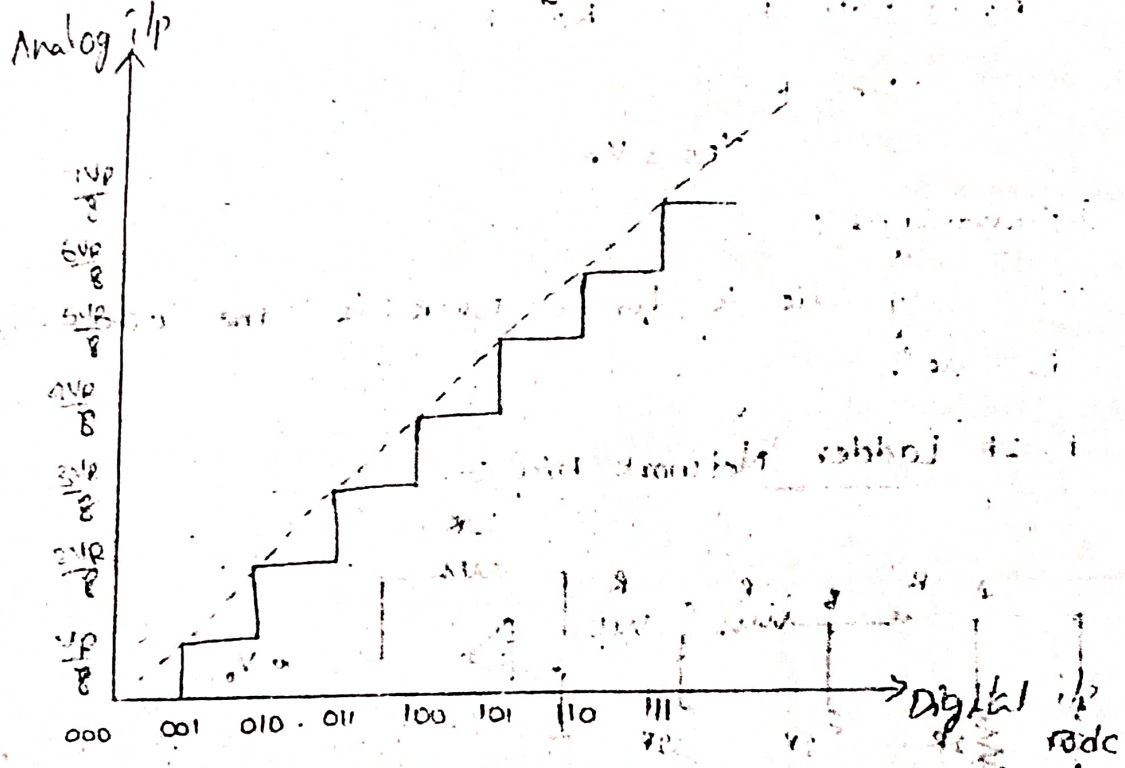
d_n = Least Significant bit (LSB) $\frac{V_{FS}}{2^n}$

There are 3 types of DAC techniques to implement the above eqn those are

1. Binary weighted resistor DAC
2. R-2R Ladder network DAC
3. Inverted R-2R DAC

Binary weighted Resistor DAC :





Binary weighted Resistor method uses n electronic switches $d_1, d_2, d_3 \ldots d_n$ Controls the i/p binary word. From the dt the switches are Single pole double through switches (SPDT). If the binary i/p is one the switch is connected to the reference voltage V_R and if the binary i/p is zero. the switch is connected to grandi.

From the fig the o/p current I_0 is calculated by using

$$I_0 = I_1 + I_2 + I_3 \cdots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2R} d_2 + \frac{V_R}{2^3R} d_3 + \cdots + \frac{V_R}{2^nR} d_n$$

$$I_0 = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

From the fig

$$V_0 = I_0 R_f$$

$$\therefore \frac{V_R}{R} \cdot R_f \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

By the comparision the above eq with the basic eqn

$$V_0 = k V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

From both the eq's $R_f = R$

then $K = 1$

$$V_{FS} = V_R$$

Disadvantages :-

The only dis is for a BWR is "the circuit complexity is more".

R-2R Ladder Network DAC :-

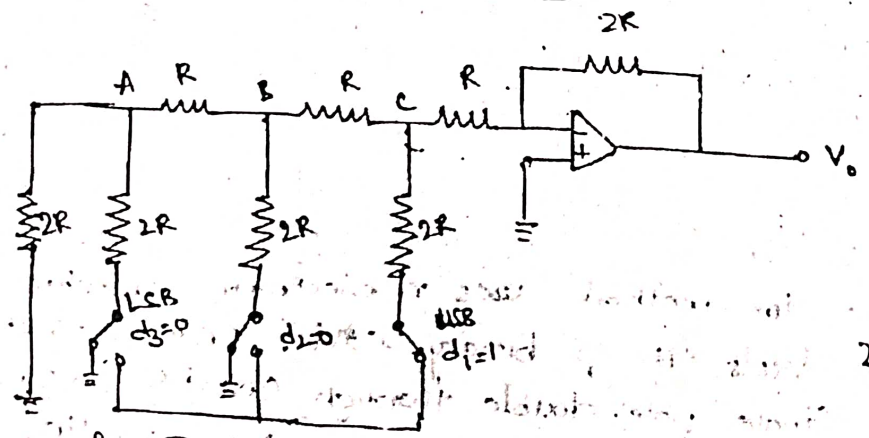
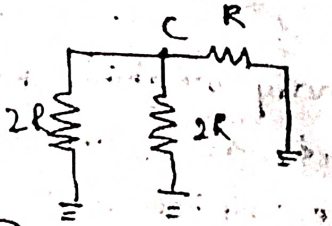
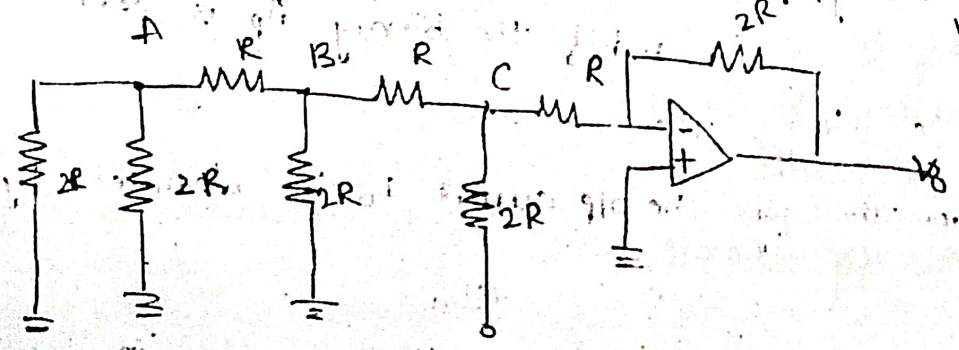


fig (a)



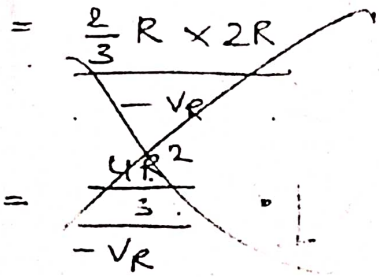
(c) Equivalent ckt at node c

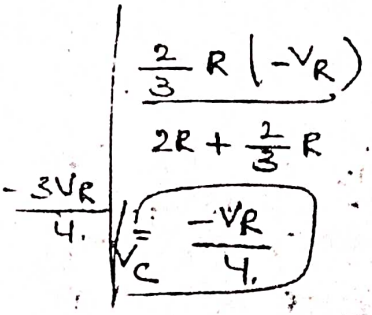


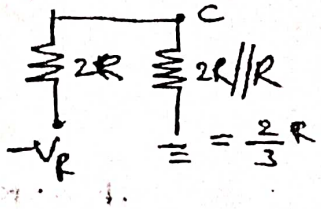
(b) Equivalent of ckt fig (a)

the wide range of resistors are required in Binary weighted resistor DAC. This problem can be avoided by using R-2R DAC by using only two values of resistors with the range of ϕ 2.5kΩ to 10kΩ. The simple understanding purpose. Consider a 3-bit DAC where the switch positions d_1, d_2, d_3 as 100. This can be simplified by using the fig(b) and finally the voltage at node c can be easily calculated by using fig(c)

i.e., voltage at node c







$$V_o = \frac{-R_f}{R_1} V_{in}$$

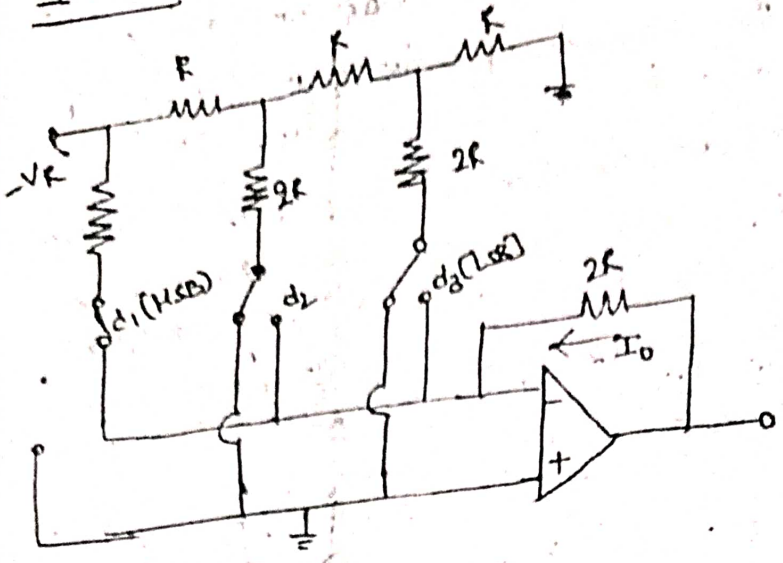
Then from the fig the o/p voltage $V_o = \frac{-2R}{R}\left(\frac{+V_R}{4}\right)$

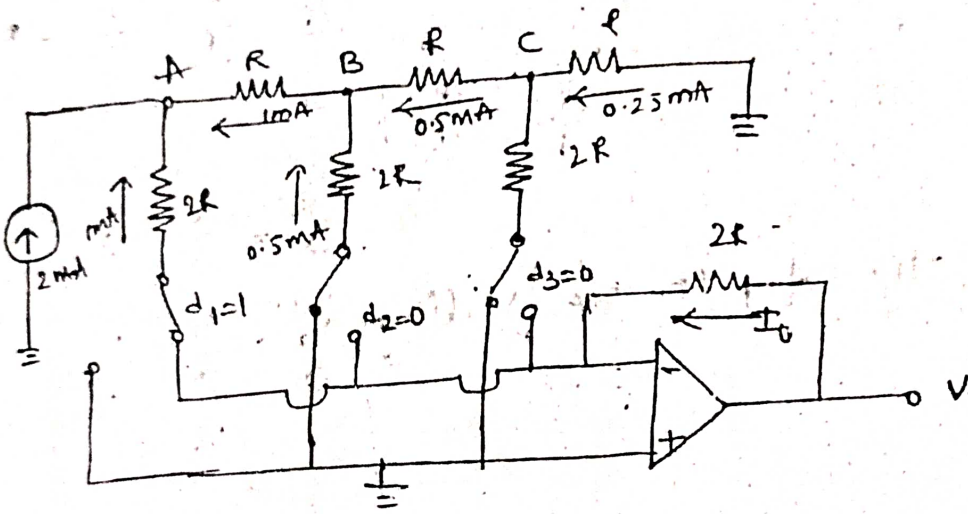
$$V_o = \frac{V_R}{2}$$

Disadvantages:

1. The current flow in the resistors changes as the i/p data changes
2. Here power consumption causes heating which produces non-linearity DAC

Inverted R-2R ladder network :-

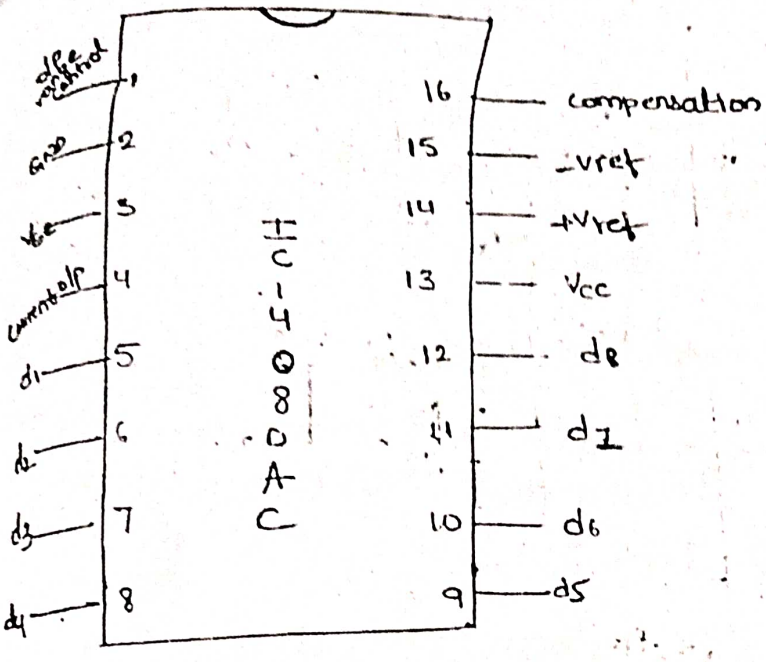




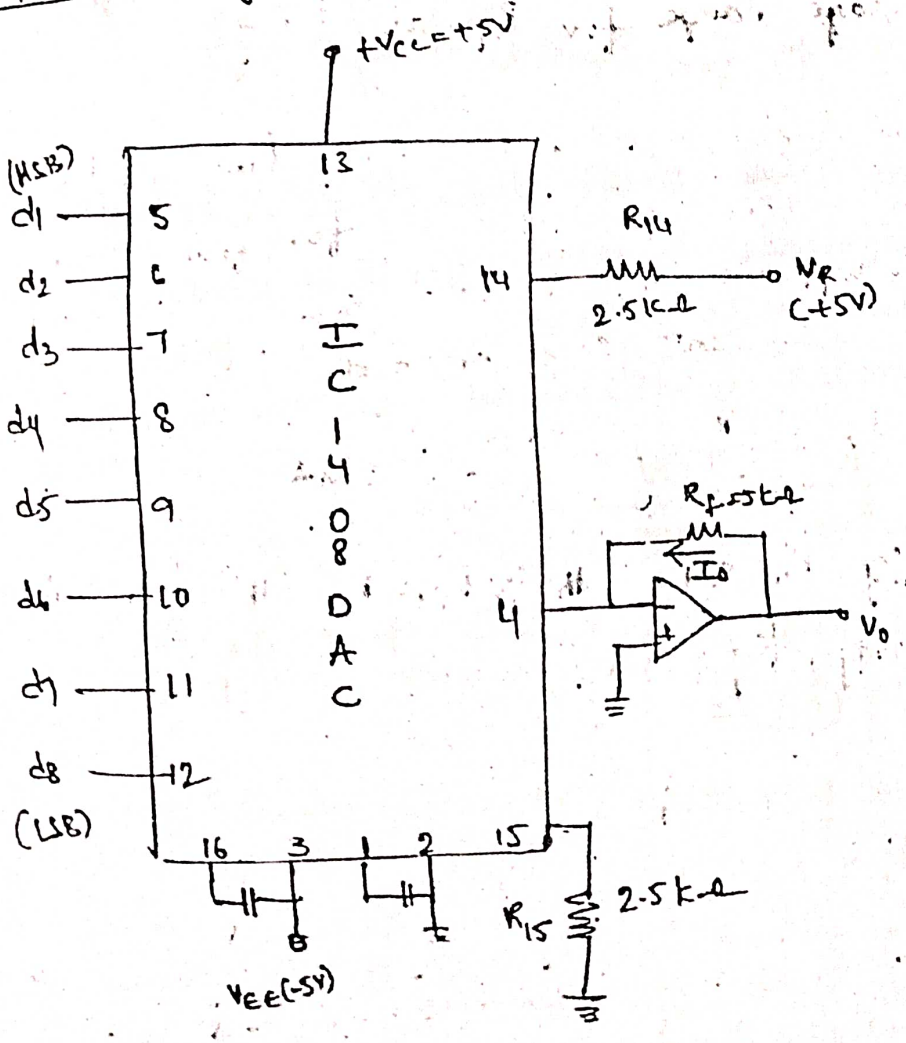
The drawbacks of BWR and R-2R ladder DAC was overcome by using inverted " " " whose switch positions was interchanged from previous ckt so it is called as inverted R-2R ladder N/W.

From fig (b) consider the reference current has 2mA. This was equally divided at node A as 1mA. Similarly this 1mA equally divided at node B as 0.5mA and also at node C it is 0.25mA

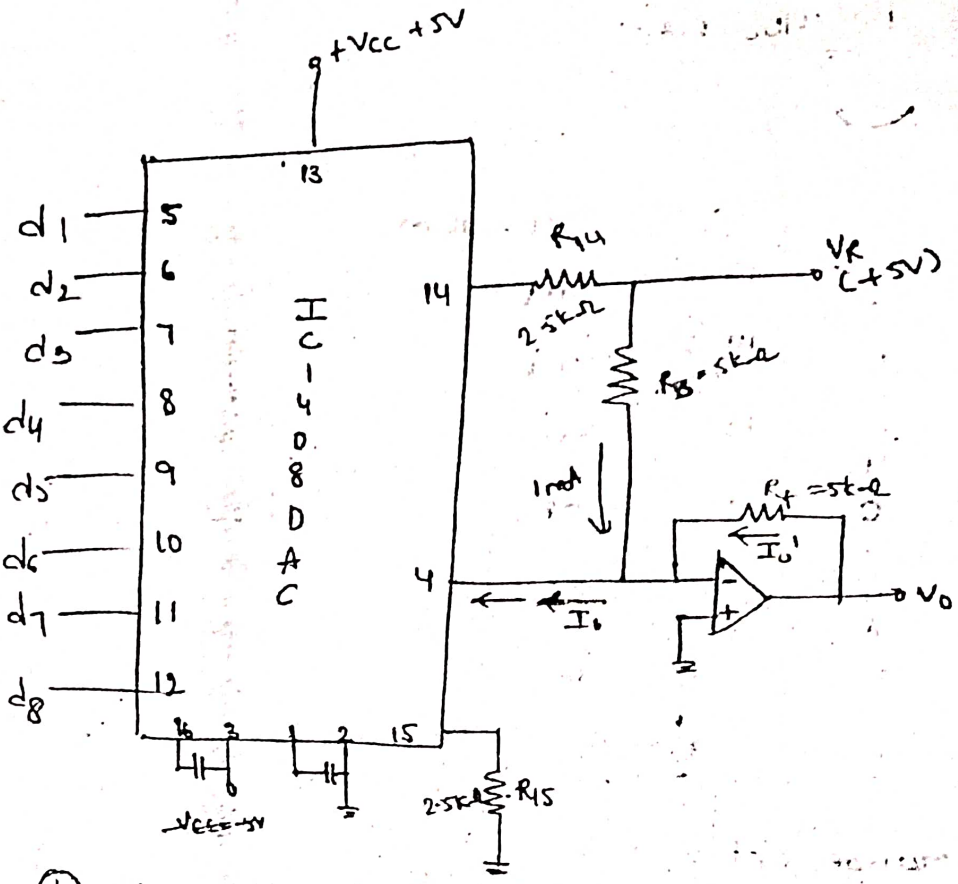
Monolithic IC 1408 DAC :-



unipolar range ckt :-



a) o/p voltage in unipolar range



(b) o/p voltage range for Bipolar Range

A typical 8-bit IC1408DAC has 8-bit data lines d_1 to d_8 It requires 2mA reference current for full scale, I/p and two power supplies $V_{CC} = 5V$ and $V_{EE} = -5V$, then the total reference current is determined by the resistor using R_{14} i.e.,

$$I_R = \frac{V_R}{R_{14}} = \frac{5V}{2.5} = 2mA$$

from the fig R_{14} & R_5 th is $R_{14} = R_5$ then I_0 is calculated by using fig (a) is

$$I_0 = \frac{V_R}{R_{14}} \left(\sum_{i=1}^{8} d_i 2^{-i} \right)$$

$$= \frac{V_R}{R_{14}} \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} + d_5 2^{-5} + d_6 2^{-6} + d_7 2^{-7} + d_8 2^{-8} \right] \quad \text{---(1)}$$

For unipolar range:

Consider all digital i/p's as 1

i.e., d_1 to d_8 - 11111111 then from eq^n ①

$$I_0 = \frac{5}{2.5k\Omega}\left[1\times 2^{-1}+1\times 2^{-2}+1\times 2^{-3}+1\times 2^{-4}+1\times 2^{-5}+1\times 2^{-6}+1\times 2^{-7}+1\times 2^{-8}\right]$$

$$I_0 = \frac{5}{2.5k\Omega}\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= I_0 = 1.99\ mA \quad | \quad V_0 = I_0 R_f$$

$$= 1.99\times 10^{-3}\times 5\times 10^{3}$$

$$\boxed{V_0 = 9.96V}$$

For bipolar range: Consider range from −5V to +5V by adding a resistor $R_B = 5k\Omega$ in b/w V_R and pin 9. From fig ⑥ the bipolar operation o/p current $I_0' = I_0 - \frac{V_R}{R_B}$

$$I_0' = \frac{V_R}{R_4}\left[d_1 2^{-1}+d_2 2^{-2}+\ldots+d_8 2^{-8}\right]-\frac{V_R}{R_B}\Big] \quad \text{—②}$$

I_0' & o/p voltage $V_0 = I_0' R_f$ —③

Let us consider the digital i/p d_1 to d_8 = 00000000

from ② $I_0' = 0 - \frac{5}{5k\Omega} = -1\ mA$

eq^n ③ $V_0 = -1\times 10^{-3}\times 5\times 10^{3} = -5V$

Let us consider the digital i/p d_1 to d_8 as = 10000000

from ② $I_0' = \frac{V}{R_{14}}\left[1\times 2^{-1}+0+0+0+0+0+0+0\right]-\frac{V_R}{R_B}\Big]$

$$= \frac{5}{2.5\times 10^{3}}\times\frac{1}{2}-\frac{5}{5\times 10^{3}} = 0$$

$I_0' = 0$

from ③ $\boxed{V_0 = 0}$

Let us consider the digital i/p d_1 to d_8 is 11111111

Then from eq^n (2)

$$I_0' = \frac{V_R}{R_4}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_8 2^{-8}\right] - \frac{V_R}{R_B}$$

$$I_0' = \left[1.99 \times 10^{-3} \div \frac{5}{5k\Omega}\right]$$

$$= 0.99\ mA$$

from eq^n (3) $V_0 = I_0' R_f$

$$V_0 = 0.99 \times 10^{-3} \times 5 \times 10^3$$

$$\boxed{V_0 = 4.95 \simeq 5V}$$

problem :

(1) An 8 bit DAC has an o/p voltage range 0 to 2.55 Volts. Define its resolution and Calculate % of resolution. Resolution is defined as the ratio of full scale voltage (V_{FS}) to the least bit of n-bit a DAC ($2^n - 1$) i.e.,

resolution = $\frac{V_{FS}}{2^n - 1}$

$$= \frac{2.55}{2^8 - 1} = 0.01$$

(2) The LSB of a 10 bit DAC is 20 mV calculate its (i) % of resolution (ii) full Scale range (iii) o/p voltage for 1011001101

% Resolution = $\frac{V_{FS}}{2^n - 1}$

$$= \frac{20 \times 10^{-3}}{2^{10} - 1} = 0$$

% = 1.95 ≃ 2%
devol

(ii) Full scale range is V_{OFS} = Fullscale − % resolution

$= 20\times10^{-1} - \frac{2}{100}$ [2%]

$= 20\times10^{-1} - 0.02$

$= 0.002 - 0.02$

$= 0$

Then the range is 0 to 20 mV

(iii) o/p voltage

$V_o = k V_{FS} \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} + d_5 2^{-5} + d_6 2^{-6} + d_7 2^{-7} + d_8 2^{-8} + d_9 2^{-9} + d_{10} 2^{-10} \right]$

$V_o = 1 \times 20\times10^{-3} \left[1\times2^{-1} + 1\times2^{-3} + 1\times2^{-4} + 1\times2^{-7} + 1\times2^{-8} + 1\times2^{-10} \right]$

$V_o = 20\times10^{-3} [$

(3) How many bits are required to design a D/A convertor that can have a resolution of 5 mV with 8 V full scale.

Resolution $= \frac{V_{FS}}{2^n - 1}$

$5\times10^{-3} = \frac{8}{2^n - 1} \Rightarrow 2^n - 1 = \frac{8}{5\times10^{-3}}$

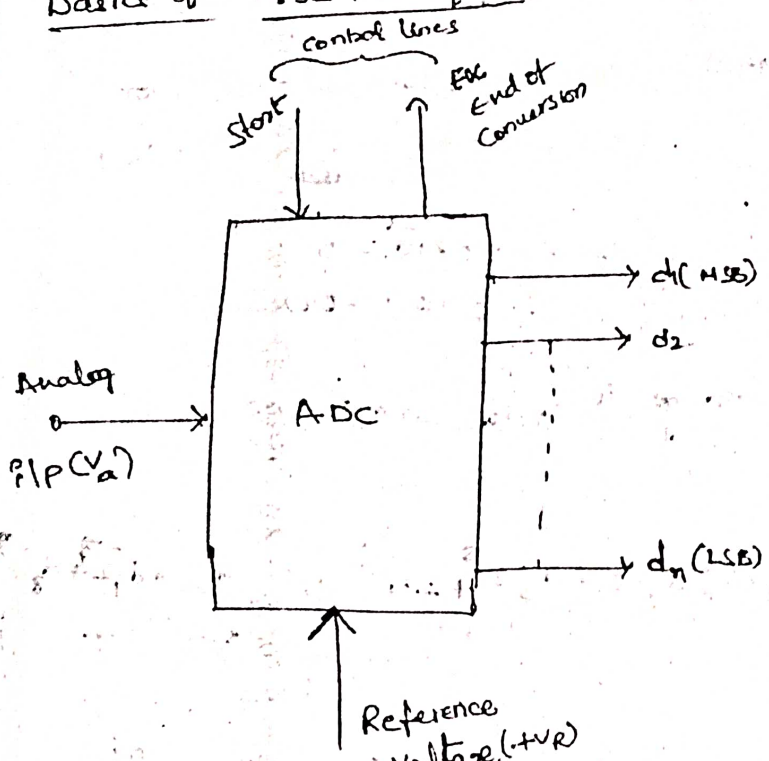
$2^n = \frac{8}{5}\times10^3 + 1$

$2^n = 1601$

$2^n = 2^{11}$

$n = 11$

Basics of A/DC Techniques:-

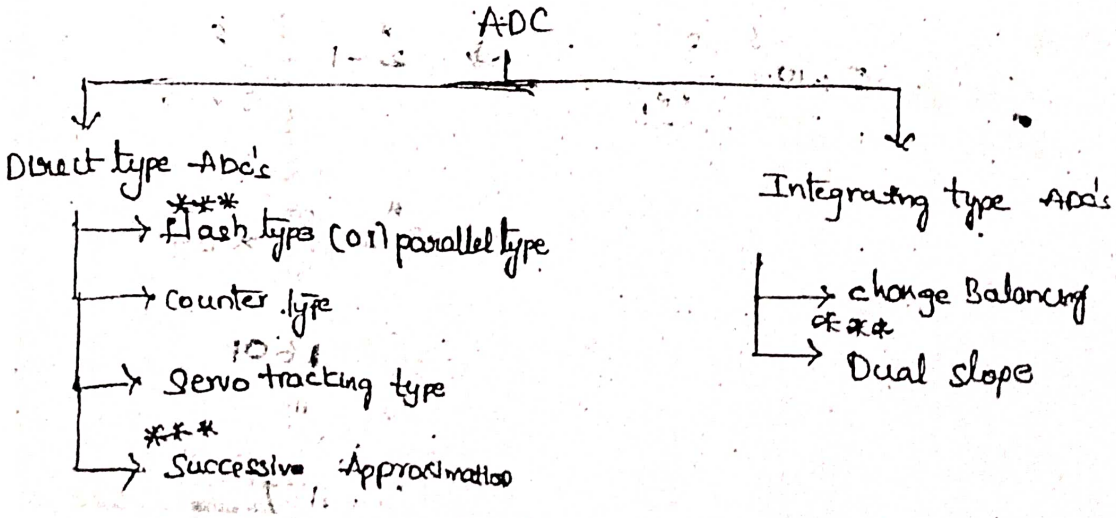


The A/D convertor exactly opposite to Digital to Analog Convertor which produces the o/p as digital mode i.e,

$$D = [d_1 2^{-1} + d_2 2^{-2} + \cdots d_n 2^{-n}]$$

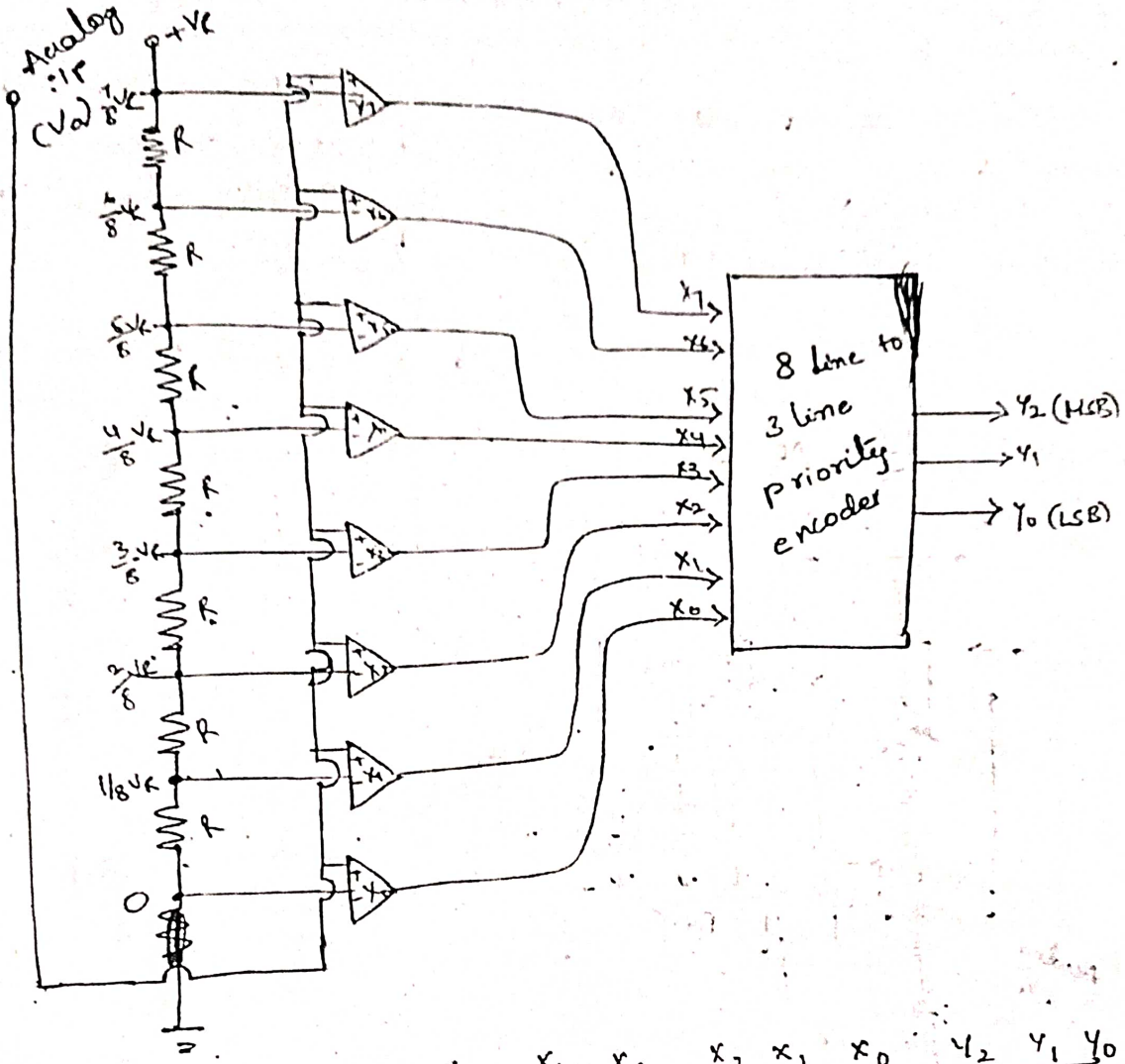
In this A/D convertor when the conversion is started it is executed by start control line and when the conversion is completed the end of conversion (EOC) control line is used

Classification of ADC:-



Direct type ADC:

① Flash type (or) parallel type:



I/p voltage	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	0	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

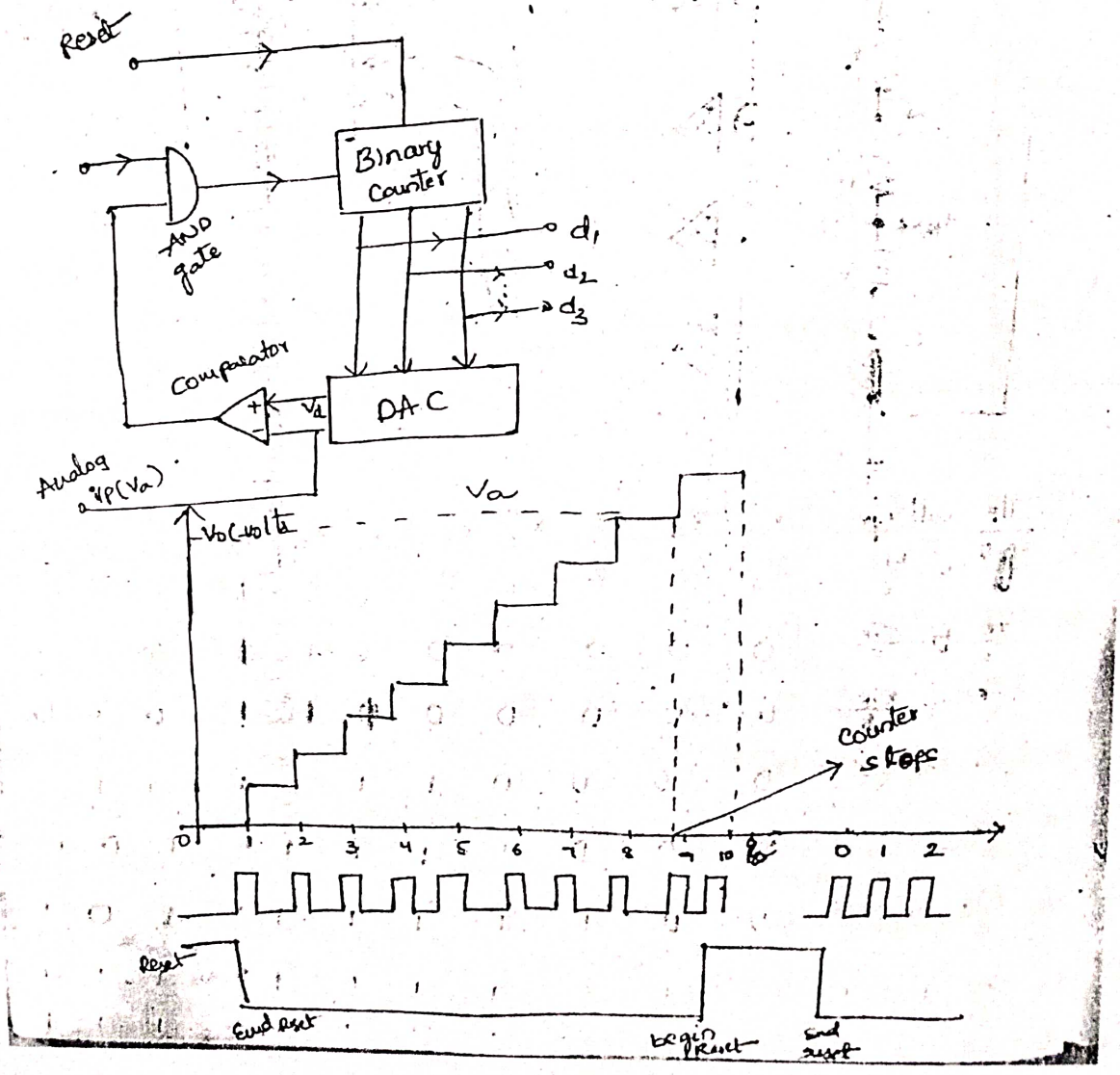
In this flash type A/D convertor is the fastest technique and most expensive. The ckt consists of a resistive divider network, 8 op-amp comparators and priority encoder is used. 8×3

This type of convertor has the disadvantage that no. of op-amps requires almost doubles. If the analog i/p $V_a > V_R$ then it gives the higher value otherwise it gives lower value i.e., $V_a > V_R \Rightarrow V_0 = 1$

$V_a < V_R \Rightarrow V_0 = 0$

$V_a = V_R \Rightarrow V_0 = 0$ (or) 1

② Counter type ADC's :-

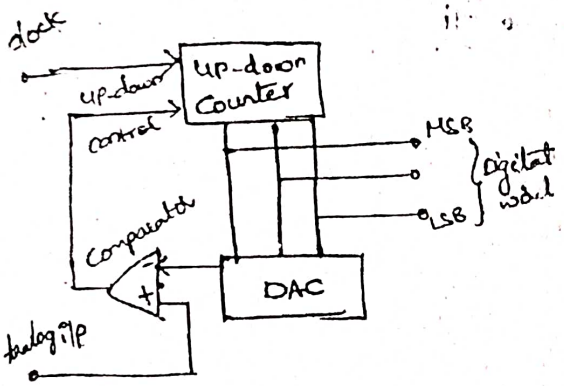


This is based on 'n' width counting principle. The counter is reset to zero by the reset pulse, when the reset was released the clock pulses was counted by the binary counter these pulses go through and gate which is enabled by the voltage comparator high o/p.

If the analog i/p (V_a) is greater than DAC converter(V_d) comparator becomes high and the AND gate is enabled to allow Txsion of clk pulses to the counter

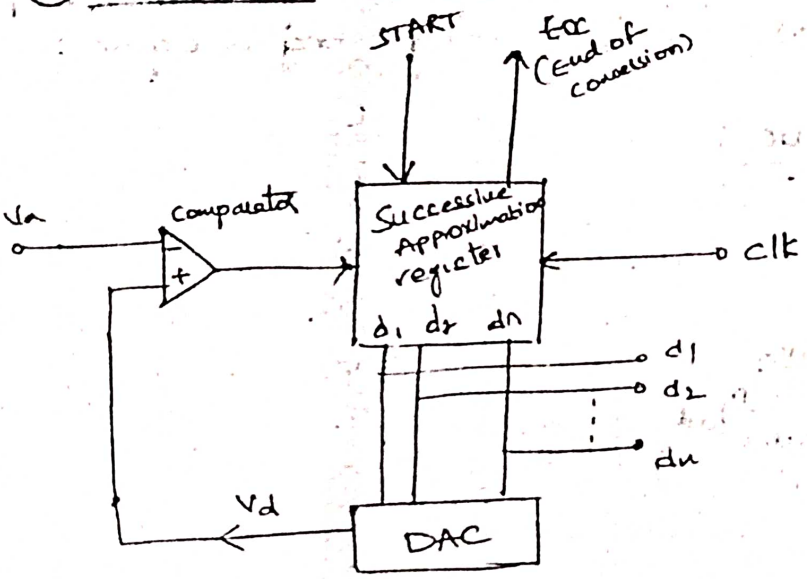
If $V_a < V_d$ the o/p of comparator becomes low and AND gate is disabled and the counter stops counting when $V_a \leq V_d$ then the end of reset and counting begins again.

3. Servo tracking type A-DC :-



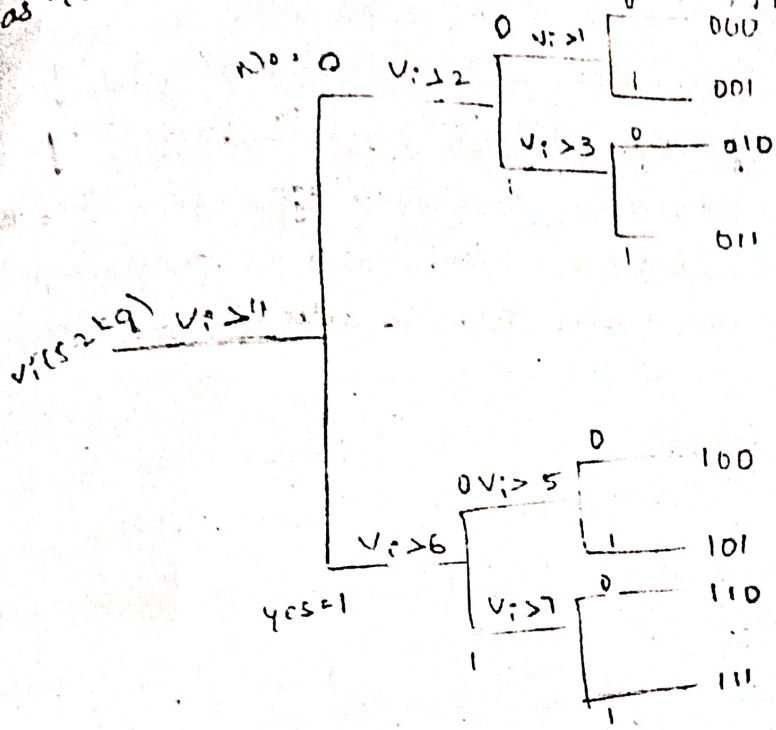
The servotracking ADC consists of up-down counter to count the no. of clock pulses of up-down → if the i/p $V_a > V_d$ the o/p of the comparator goes high and counter is counts only up pulses the digital to analog convertor o/p increases with each incoming clk pulses and then → if $V_a < V_d$ the counter counts only the down pulses. The advantage of this ADC is very simple and the drawback is more time it takes for the conversion.

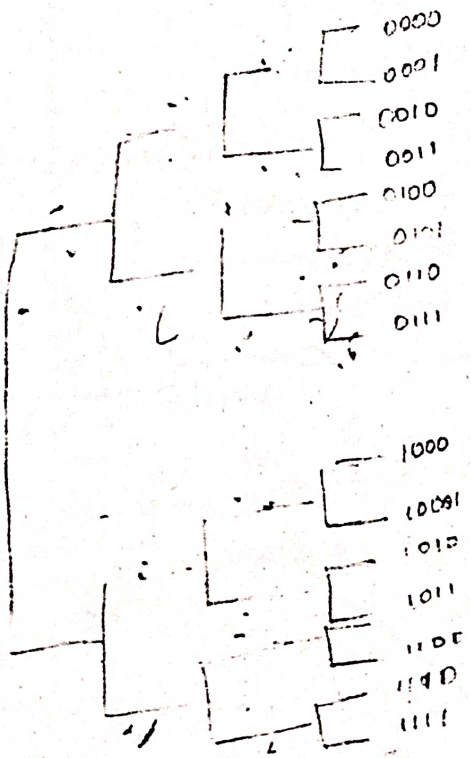
(4) Successive Approximation ADC :-



The Successive Approximation method is a n-bit of Conversion in just n-clk pulses the ckt uses Successive Approximation register (SAR) to find the required value of each bit by Trail and error method The ckt operates with the arrival of START Command. The best example is the weighing machine whenever the weights are applied as the analog i/p for one side as 5.2 kg and other side is to increase the weightages like 1kg, 3kg, 5kg & 7kg Then if $V_a > V_d$ the Successive approximation register and comparator produces a high value, otherwise low value i.e., 0

Let us consider Analog i/p as 5.2 kg. The ckt operates as follows.





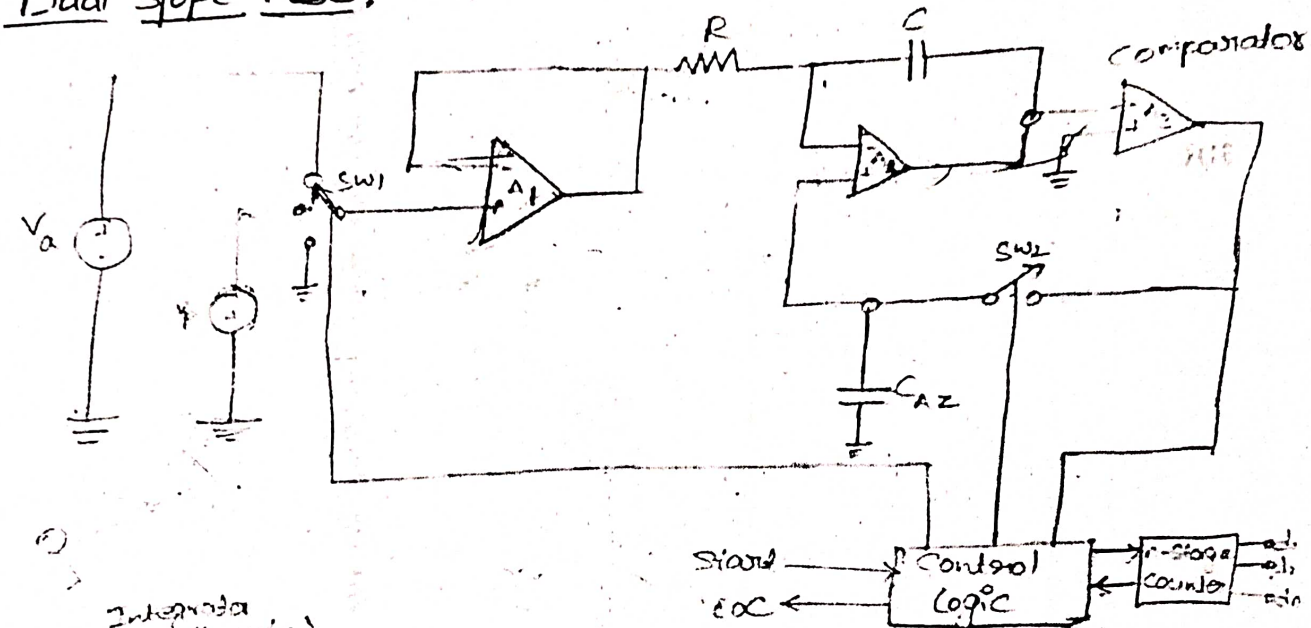
Integrating type ADC's:-

Charge balancing ADC:

The charge balancing ADC is used for ① Integrating the i/p signal to frequency by using voltage to frequency converter which is a counter which converts the voltage into freq then measure by a counter and converted into o/p is proportional to the analog i/p i.e. $f=\frac{1}{T}$ This ADC is also called as

SINGLE SLOPE ADC

Dual slope ADC:-



The dual slope ADC consists of a high i/p isolated buffer (A_1), precision integrator (A_2), voltage comparator (A_3). The convertor first integrates analog i/p signal V_{in} for a fixed time that it integrates its reference voltage ($+V_R$) with n- no. of clock cycles and analog voltage integrates 2^n clk cycles.

Before start command arrives switch-1 connects to ground and switch-2 closed. ~~Any~~ offset voltage ~~present~~ present in the A_1, A_2, A_3 the voltage appears across the capacitor (C_{Az}) (Auto zero capacitor) which provides automatic compensation for the i/p offset voltages for all op-amp's

After start command arrives at $t = T_1$, switch 2 opens by the control logic & switch 2 connects to V_a and enables the counter starting from 0. the ckt uses 'n' stage Counter and results to 0 after counting 2^n pulses. the analog voltage (V_a) is integrated for a fixed no of 2^n counts of clk-pulses. If the clk period is T then the integration takes place for a time $T_1 = 2^n T$ & the o/p is ramp going downwards.

The counter resets itself to 0 at the end of interval T & switch 1

From Fig. $T_1 = t_2 - t_1 = \frac{2^n \text{ clk pulses}}{\text{clk period}} = 2^n T$ — (1)

and

$$t_3 - t_2 = \frac{\text{Digital Count (N)}}{\text{clk period}} = NT \quad \text{—— (2)}$$

For an integrator the o/p voltage is $\Delta V_0 = \frac{-1}{RC} V(\Delta t)$

where $V_0 = V_1$ at time $T = t_2$ then it integrates the analog i/p voltage then,

$$V_1 = \frac{-1}{RC} \int V_a (t_2 - t_1) \quad \text{—— (3)}$$

I/p the -ve Reference voltage was integrated Then

$$V_1 = \frac{-1}{RC} \int (-V_R)(t_3 - t_2) \quad \text{—— (4)}$$

Now substitute the values of eq^n (1) & (2) in eq^n (3) & (4)

$$V_1 = \frac{-1}{RC} \int V_a \, 2^n T$$

$$V_1 = \frac{-1}{RC} \int -V_R \, NT$$

$$\therefore \frac{-1}{RC} \int V_a \, 2^n T = \frac{-1}{RC} \int -V_R \, NT$$

$$V_a = -V_R \frac{N}{2^n}$$

From this above eq^n if the V_R is constant then

$$V_a = \frac{N}{2^n}$$

From this eq^n we observe that if

(i) if V_R and N are constant the analog voltage is proportional to N ($V_a \propto N$)

(ii) Dual slope ADC integrates i/p signal at 2^n times of T which rejects the noise.

main disadvantage it takes long conversion time.

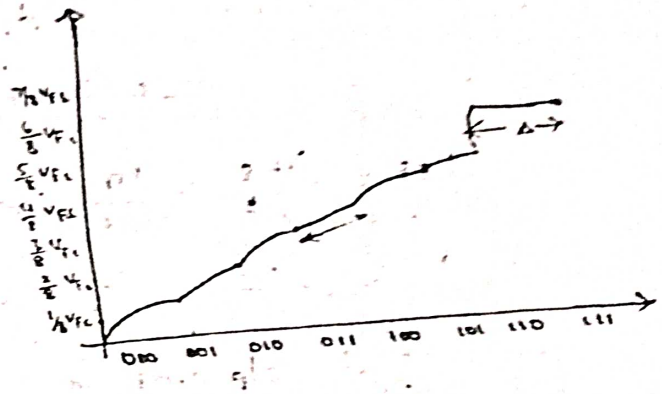
DAC / ADC Specifications

Resolution ② Linearity ③ Accuracy ④ Monotonicity ⑤ Settling time ⑥ Stability.

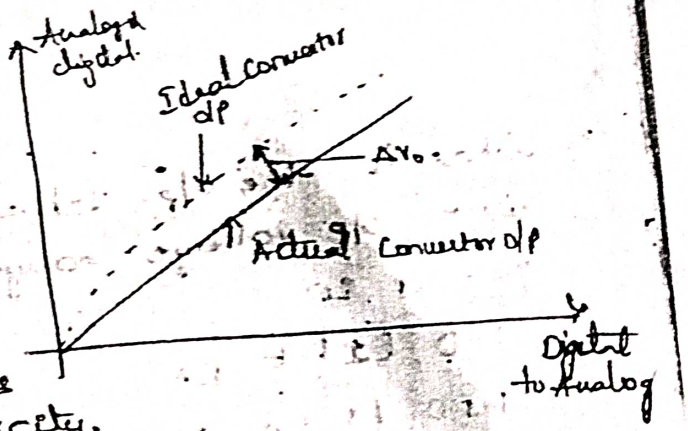
① **Resolution**: It is defined as the smallest change in voltage which may be produced at the o/p of the convertor i.e.,

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

② **Linearity**: The linearity of an A/D & D/A convertor is an improvement if its accuracy and linearity tells how close the convertor o/p but when ever one i/p increases the respective o/p increases as linearly



③ **Accuracy**: The absolute accuracy is defined as the max deviation b/w actual convertor o/p & ideal convertor o/p.



④ **Monotonicity**: It is defined as when the ↑es or ↓es the o/p is also ↑ or ↓ constant o/p was produced. It is called as Monotonicity.

⑤ **Settling time**: It is defined as the time taken for to settle with in the specified band ±1/2 LSB of its final value.

⑥ **Stability**: The performance of the convertor changes with age, power supply variations: all relevant parameters such as off set error gain error, linearity error, Monotonicity all these values are stable with any changes was produced.

Problems

1. The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 volts what is the o/p for 101101111.

Sol: $V_0 = k V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4} + \dots + d_9 2^{-9}\right]$

$= 1 \times 10.3 \times 10^{3}\left[1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + \dots + 1 \times 2^{-9}\right]$

$V_0 = 7.38$ mV

2. calculate the value of LSB, HSB & full Scale o/p for an 8 bit DAC with in 0 to 10V range

$$V_0 = k V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + \dots + d_8 2^{-8}\right]$$

$$= V_{FS}\frac{d_1}{2} + \frac{d_2}{2} V_{FS} + V_{FS}\frac{d_3}{2^3} + \dots + \frac{d_8}{2^8} V_{FS}$$

$$LSB = \frac{V_{FS}}{2^8} = \frac{10}{2^8} = 0.39\,V$$

$$HSB = \frac{V_{FS}}{2^1} = \frac{10}{2^1} = 5V$$

Full scale o/p voltage = full scale range − LSB

$= 10 - 0.39$

$= 9.961V$

3. what is the o/p voltage produced by D/A convertor whose o/p voltage range is (0-10)V & whose i/p binary number is

(i) 10 (2 bit DAC)

(ii) 0110 (4 bit DAC)

(iii) 10111100 (8 bit DAC)

(i) 10 (2 bit DAC)

$$V_0 = k V_{FS}\left[d_1 2^{-1} + d_2 2^{-2}\right]$$

$$= 1 \times 10\left[1 \times 2^{-1} + 0 \times 2^{-2}\right]$$

$$= 10\left(\frac{1}{2}\right)$$

$= 5V$

(ii) 0110

$V_0 = kV_{fs}\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right)$

$= 1 \times 10\left(0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4}\right)$

$= 3.75V$

(iii) 10111100

$= 1 \times 10\left(1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6} + 0 \times 2^{-7} + 0 \times 2^{-8}\right)$

$= 7.34V.$