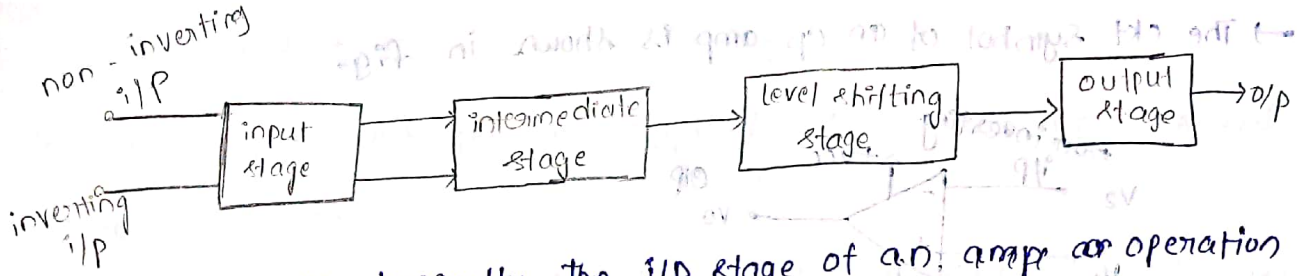
# Unit-2

## Operational Amplifier

### operational amplifier (or) Typical amplifier:-




→ A diff amp is basically the i/p stage of an amp or operation amp.

→ An operational amp abrivatated as op amp is versatile electronice device which finds to many ap practical applications.

→ An operational amp is basically very high gain direct coupled amp with high i/p impedence and low o/p impedence.

→ the block diagram of op-amp as shown in fig. from the block diagram it is seen that the i/p stage employes a dual i/p balanced o/p stage. diff amp which provides a major parts of the voltage gain and high i/p resistance.

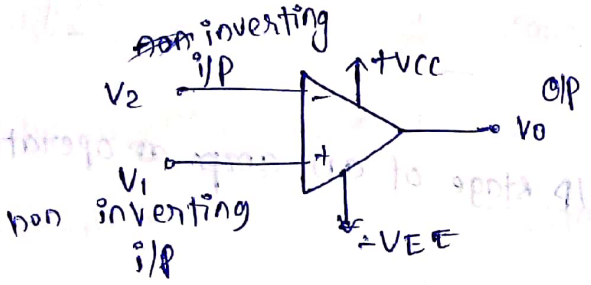
→ This can be applied intermediate stage which is another dual i/p balanced o/p diff amp. Since the i/p stage amp and intermediate stage amp are direct coupled. So the DC voltage at the o/p of an intermediate stage gives rise to above the ground which is not desirable.

→ ∴ To bringing the DC voltage down to '0'. A level shifter (or) translator is used this is usually an emitter follower. It acts

as buffer with large i/p impedence and low o/p impedence.

→ The o/p stage contains a complementary symmetry push pull amp which helps to increase the o/p voltage swing. and the current supplying capacity of an op-amp.

→ The ckt symbol of an op-amp is shown in fig.




→ let the i/p voltages $V_1$ and $V_2$ we apply at the noninverting and inverting terminals respectively of an op-amp let $V_0$ denotes an o/p voltage we have

$$V_0 = A(V_1 - V_2)$$

where A is the diff gain of an op-amp.

→ If the inverting i/p terminal is grounded

ie, $V_2 = 0$ and the voltage $V_1$ is applied then we have $V_0 = AV_1$

→ Similarly the non inverting i/p terminal is ground i.e, $V_1 = 0$ the voltage $V_2$ is applied the then have

$$V_0 = -AV_2$$

## Characteristics of ideal and practical op-amp:-

→ An ideal op-amp exhibits the following characteristics

i) voltage gain is 'ꝏ'

ii) The i/p impedence is 'ꝏ'

iii) The o/p impedence is '0'

iv) The B.w is 'ꝏ'

→ When equal voltages are applied at the two i/p terminals the o/p is zero.

→ There is no change in the characteristic features with changes of temperature.

→ where as in practical op-amp the voltage gain is large and very high i/p impedence and very low o/p impedence

→ A small o/p voltage appears even when equal voltages are applied at the ~~two~~ two i/p terminals.

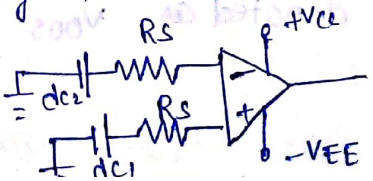
## i/p offset voltage:-

→ It is defined as the voltage that needs to be applied across the i/p terminals of an op amp in order to cause the o/p voltage to becomes zero.

→ In other words it is the voltage which must be applied b/w the inverting and non inverting terminals to null the o/p.

→ It is denoted as '$V_{io}$'

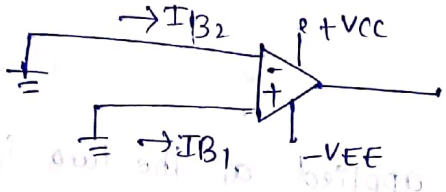
→ It is generally in the order of few microvolts.




$V_{io} = V_{dc1} - V_{dc2}$

## I/p OFF set current:

→ It is defined as the algebric difference b/w the currents into the inverting and noninverting i/p terminals of an op-amp. It is denoted by '$I_{io}$'.




$$I_{io} = |I_{B1} - I_{B2}|$$

→ Let $I_{B1}$ and $I_{B2}$ denote the currents which flow into the i/p terminals in the transistors are properly biased.

→ where $I_{io}$ is the order of few nano amperes.

I/p bias current:-

→ It is defined as the mean of the current that flow into the inverting and noninverting terminals of an op-amp. It is denoted by '$I_B$'.

→ It is usually in the order of few nano amperes.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where $I_{B1}$ and $I_{B2}$ are the base currents of the transistors of the 1st stage.

O/p Offset voltage:-

The voltage which appears as o/p for '0' i/p, is termed as o/p offset voltage. It is denoted as '$V_{oos}$'.

Slew rate :- It is defined as the max rate of change of o/p voltage for unit time.

$$SR = \left.\frac{dv_o}{dt}\right|_{max} \quad V/\mu sec$$

→ The slew rate of an op-amp is an important parameter it is a measure of ability of op-amp to handle varying signals.

Supply voltage Rejection ratio (SVRR) (or) power supply RR (or) PSRR

It is defined as the ratio of change in i/p off set voltage to the change in supply voltage is termed as supply voltage rejection ratio.

$$SVRR = \frac{\Delta V_{io}}{\Delta V} \quad \mu V/V$$

→ since large changes i/p and off set voltages effects the performance of op-amp. So it is desirable at SVRR as low as possible.

→ It can be also expressed in 'dB'

$$SVRR = 20\log_{10}\left(\frac{\Delta V_{io}}{\Delta V}\right) \quad dB$$

drift (or) thermal drift :-

→ Bias current, off set current, off set voltage change with temperature. A ckt carefully nulled at 25°C. may not remain so when the temperature rises to 35°C this called drift.

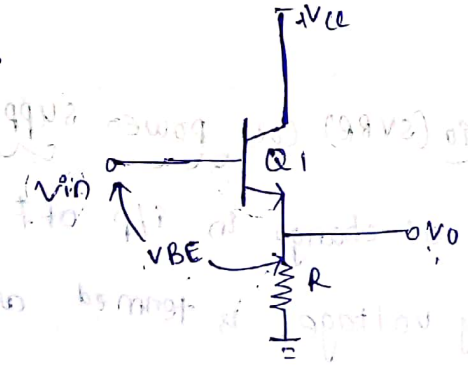
→ often i/p offset current in nanoamperes/°C

The offset voltage drift measured in μV/°C.

Level translator (or) level shifter:-

→ The level translator is basically an emitter follower

Case1:- In this case the simplest version of level translator which consists of an emitter follower with fixed resistor R in the emitter ckt.




→ let Vin denotes the DC voltage level of the o/p of intermed stage preceding level shifter stage.

→ If $V_o$ is o/p voltage we have $V_o = V_{in} - V_{BE}$

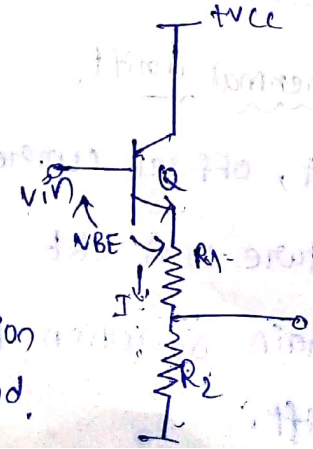
$V_o = V_{in} - 0.7$

→ By using level shifter the DC level can be brought down by abo 0.7V.

case2:- In practice the reduction of DC voltage level may prove to be impossible. In order to further bring down the volta level to practically '0'. The above ckt is modified as show in figure.

→ Resistor R is replaced by resistors $R_1$ and $R_2$ joined as shown in figure.

→ The o/p is taken b/w the junction point of $R_1$ & $R_2$ and the ground.



→ By aproper selection of $R_1$ and $R_2$, $v_o$ can be made equal to $v_i$.

→ let 'I' denotes the current through resistor $R_1$ by applying KVL to the base emitter loop of transistor Q.

$$v_{in} - V_{BE} - I(R_1+R_2) = 0.$$

$$v_{in} - V_{BE} = I(R_1+R_2) \Rightarrow \boxed{I = \frac{v_{in} - V_{BE}}{R_1+R_2}}$$

We have $V_o = I R_1$ (or) $I R_2$

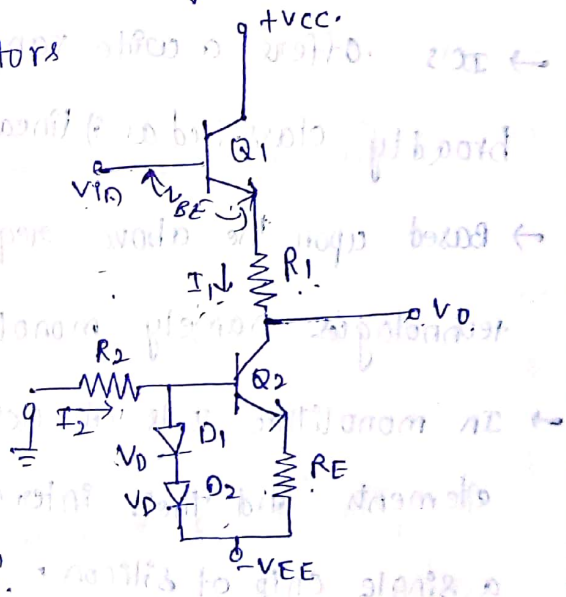
$$\boxed{V_o = \frac{R_1}{R_1+R_2}(V_{in} - V_{BE})}$$

→ Here there is a inheriant drawback it is the i/p signal gets attenuated by the factor $\frac{R_1}{R_1+R_2}$

Case 3:

→ A modified version of level translator ckt which uses a constant current source is shown in fig.

→ The transistor $Q_2$ along with resistors $R_2$ and $R_E$ and the diodes $D_1$ & $D_2$ consists a constant current source




from the ckt we have

$$V_o = v_{in} - V_{BE} - i_1 R_1$$

→ By suitable choosing the $R_1$, $R_2$ and $R_E$. The voltage $v_o$ can be broad down to '0'.

Case 4:- An improved version of a level translator ckt using current mirror as shown in fig.

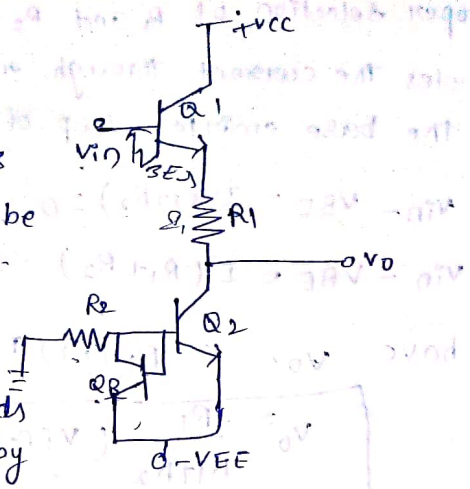
→ In the transistors $Q_2$ and $Q_3$ along with resistor $R_2$ consist current mirror arranging supply a constant current $I_1$ is shown in fig.

we have $I_1 = I_2$

and $V_o = V_{in} - V_{BE} - i_1 R_1$

→ By selecting suitable values for $R_1$ and $R_2$, the voltage can be broad down to zero level.

→ In additions to these cases there are many other methods employing different ckts by which the DC voltage level $V_o$ can be reduced to '0'.




Defination of IC :-

→ The IC is low cost electronic ckt consisting of active and passive ~~elements~~ components that are joint together on a single crystal chip of silicon.

→ ICs offers a wide range of applications, to b should be broadly classified as 1) linear ICIs 2) digital ICIs

→ Based upon the above requirements two different IC technologies namely monolithic technology and hybrid technology

→ In monolithic ICIs all ckt components both active and passive elements and their interconnections are manufactured into a single chip of silicon.

→ The monolithic ckt is used for applications where identical ckts are required in very large quantities and hence provides lowest unit cost and highest order of Availability

→ In hybrid ckts seperate component parts are attached to a ceramic substrate and interconnected by means of

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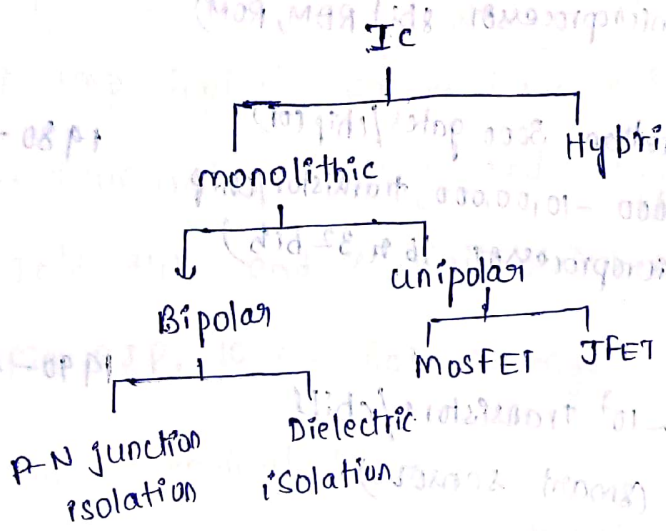
either metalisation pattern (or) wire bonds. This technology is more useful to small quantity custom ckts.

→ Based upon active devices used Ic's can be classified as Bipolar and unipolar.

→ Bipolar and unipolar Ic's may further classified as depending on the isolation technique (or) type of FET used.




Ic size and ckt complexity:-

→ upto 1950 the electronic device ~~was~~ technology was dominated by vaccume tubes

→ The present day electronics is result of invention of transistor in 1947.

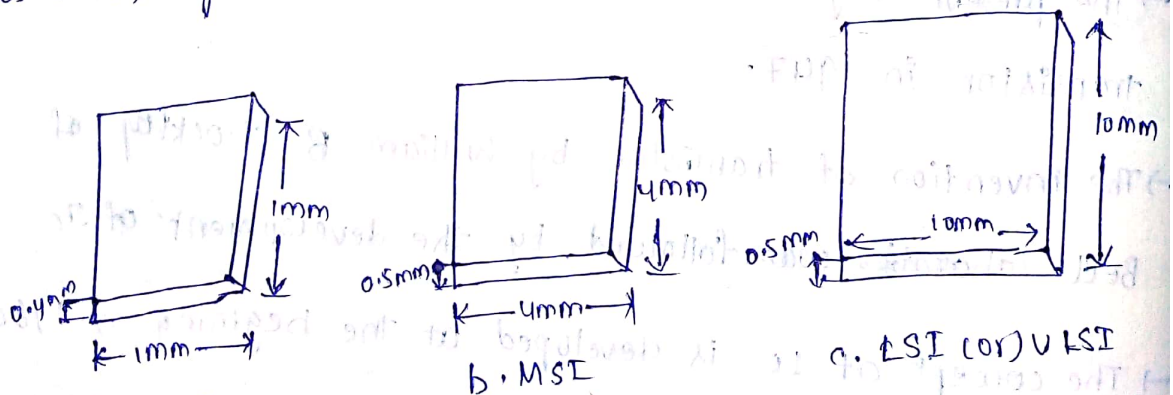
→ The invention of transistor by William B shockley of Bell Laboratories was followed by the development of Ic

→ The concept of Ic is developed at the begining of 1960 by both Texas instrument and fairchild semiconductor

→ since the time, size and complexity of the Ic are increasing rapidly as shown below.

| | | |
|---|---|---|
| First IC, SSI (Small scale integration) | 3-30 Gates/chip or 100 transistors/chip (logic gates, FF) | 1965 - 197 |
| MSI (medium scale integration) | 3-300 gates/chip (or) 100 - 1000 transistor/chip (Counters, multiplexers) | |
| LSI (large scale integration) | 300 - 3000 gates/chip (or) 1000 - 20000 transistor/chip (microprocessor 8bit RAM, ROM) | 1970 - 198 |
| VLSI very large scale integration | more than 3000 gates/chip (or) 20000 - 10,00,000 transistor/chip (microprocessor 16 & 32 bits) | 1980 - 90 |
| ULSI ultra | $10^6 - 10^7$ transistors/chips (smart sensors) | 1990 - 200 |
| GSI Giant scale integration | $> 10^7$ transistors/chips (embeded systems) | |

→ The area of the chip size for SSI and MSI and LSI (or) VLSI as shown fig.




a. SSI b. MSI c. LSI (or) VLSI

packages:-

Ic packages there are three popular available packages.

1. metal can packages.
2. Dual In line (DIP)
3. Flat package.

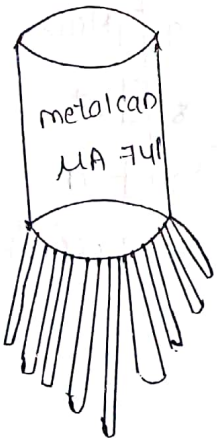
→ op-amp packages may contains single, dual, four op-amp tipical packes have 8 terminals, 10 terminals, 14 terminals, widely used very popular.

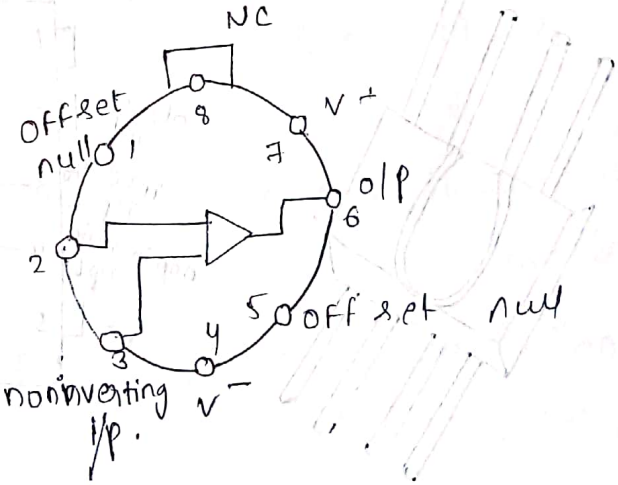
→ Ic's 741 and is available has 8 pin metal can, 8 pin DIP, 10 pin flat package.

op-amp terminals:-

→ op-amp have 5 basic terminals, i.e, 2 i/p terminals one o/p terminal and two power supply.

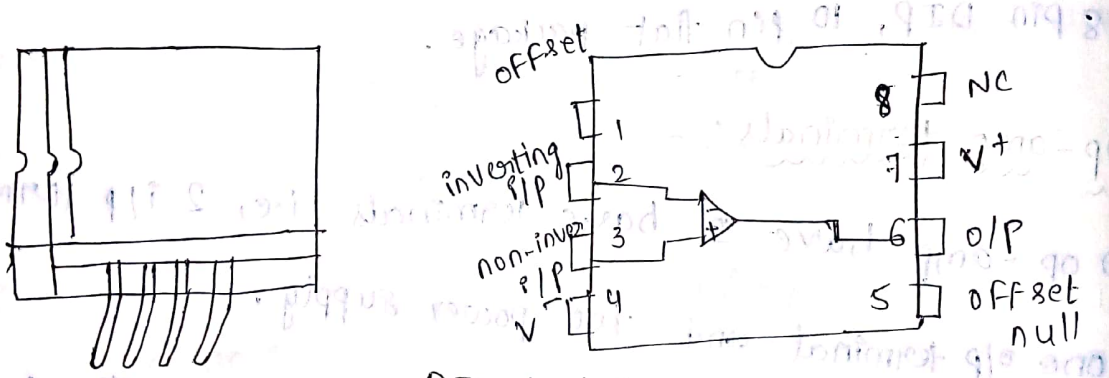
→ The significance of other terminals varies with the type of op-amp. the metal can package Ics are 741 as shown in figure.



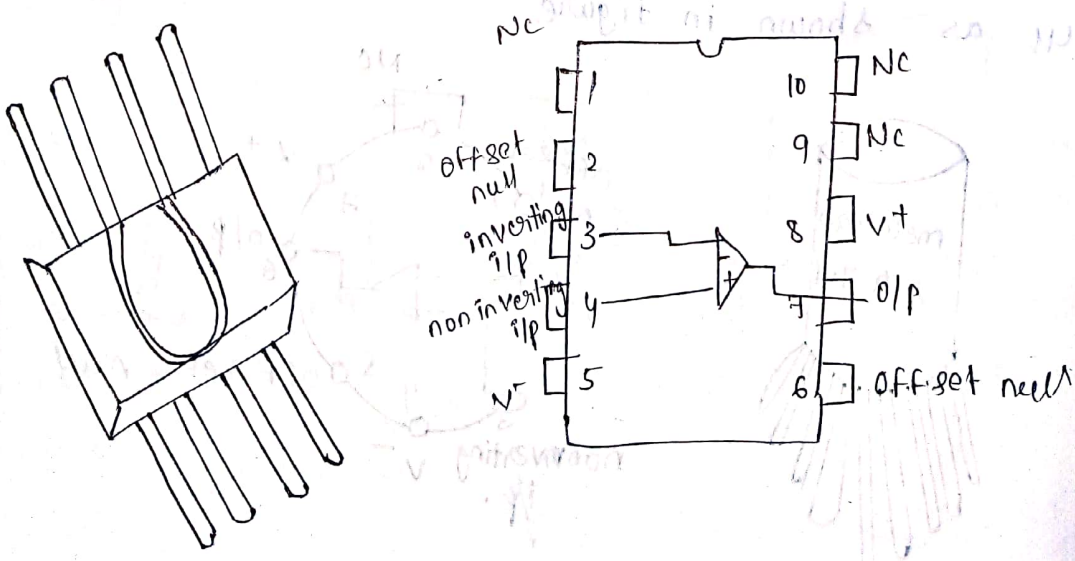
→ The metal can package top view of IC741 has a 8 pins, The pin number 8 . identified by tap. The other pin are number counter clockwise from pin 8 begining with pin 1, pin 2 is called the inverting input terminals . pin 6 is the o/p terminal and the pin 4 & 7 Vcc power supply terminals . labelled as $V^+$ & $V^-$ respectively terminals 1 & 5 are used for Dc offset The pin 8 marked as NC indicates No connection .

→ The IC 741 DIP Package as shown in figure.

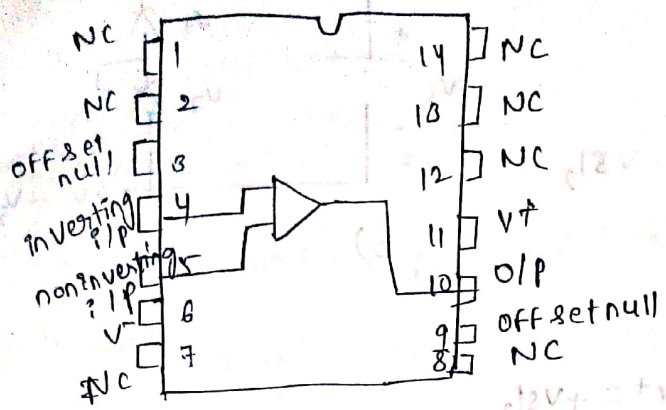



8 pin IC 741 DIP package

→ A pin 10 pin flat package shown in fig.

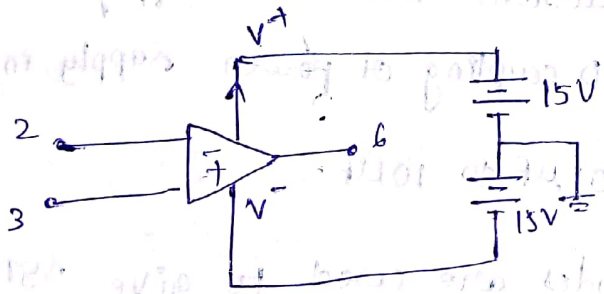



10 pin flat package



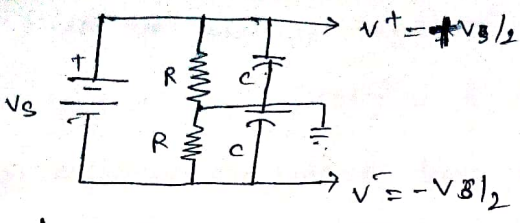

power supply connection:-

→ The $V^+$, $V^-$ power supply terminals are connected to 2 DC voltage sources. The $V^+$ pin connected to the +ve terminal of 1 source. The $V^-$ terminal is connected to -ve terminal of another source.

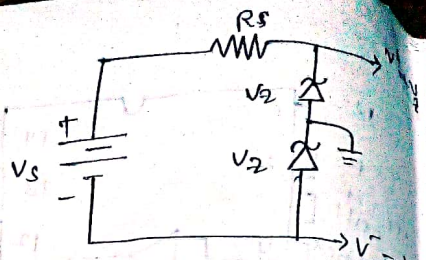



→ From the figure the two sources are 15V batterys each. These are the typical values but in general the power supply voltage may range from ±5V to ±22V.

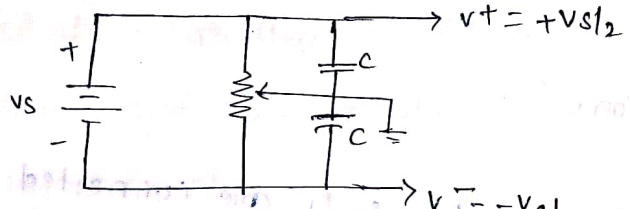
→ The common terminal of the $V^+$ and $V^-$ sources is connected to ground instead of using 2 power supplies we can use 1 single power supply we obtain $V^+$ and $V^-$ as shown in ckt.




a)




b)




c)

→ From figure (a) the resistor R should be greater than 10kΩ. so that It doesnot draw more current from the supply voltage $V_S$. The 2 capacitors provide D coupling of power supply in the range of capacitor 0.01μf to 10μf.

→ from ckt (b) zener diodes are used to give symmetrical supply voltages. The value of the Rs is choosen such that it supplies sufficient currents from the zener diodes to operate in the avalaunche mode.

→ From fig (c) potentiometer is used to get equal values of $V^+$ and $V^-$ the diodes $D_1$ and $D_2$ is used to protect the IC.

Temperature ranges:-

→ For military applications the operating temperature range $-55^{\circ}C$ to $+175^{\circ}C$.

→ In commercial applications the operating temperature range 0 to $70^{\circ}C$ / $75^{\circ}C$.

manufacturing designation:-

→ Each manufacturer uses specific code and assign a specific type number to the IC produce.

→ For example 741 can internally compensated op amp originally manufactured by fairchild semiconductors is sold as µA741

→ Here µA represents the identifying intials used by fair child.

→ The codes used by some of the well known manufactures of linear IC's are

1. fair child µA, µAF
2. National semiconductors LM, LH/LF.
3. motorola MC, MFC.
4. RCA CA, CD.
5. Signals signetics N/S, NE/SE
6. Texas Instrument SN
7. Burr-Brown. BB

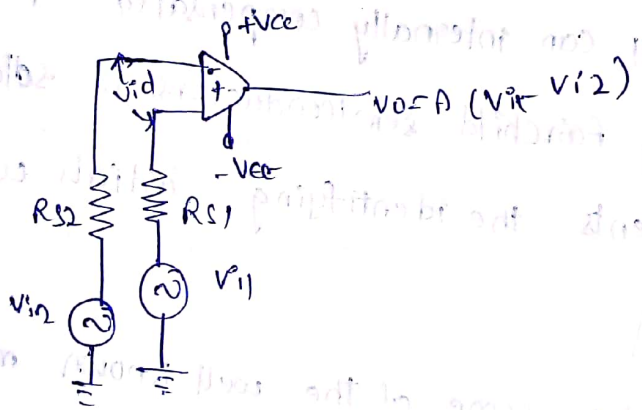
## open loop op-amp configuration:-

→ open loop means there is no interconnection b/w i/p and o/p terminals ie, there is no feedback from o/p to the i/p.

→ The open loop op-amp configurations can be widely categorized into 3 types.

1. Differential amp
2. inverting amp
3. noninverting amp

### 1. Diff amp:-

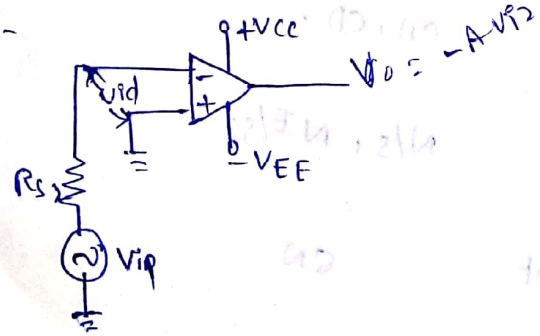



→ let $V_{i1}$ and $V_{i2}$ represents the i/p signal of inverting and noninverting i/p terminals. we have the o/p voltage $V_0 = A(V_{i1} - V_{i2})$

where A represents open loop op amp gain.

where $V_{id} = V_{i1} - V_{i2}$

### 2. inverting amp:-



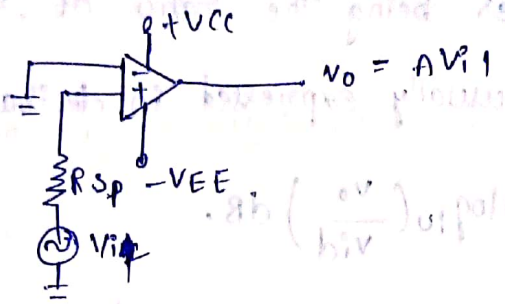

→ let the noninverting i/p terminal be grounded i.e $V_{i1} = 0$

we have the o/p voltage $V_0 = -A V_{i2}$

→ From this relation we can said that there is phase ~~relation~~ inversion

AC and DC characteristics :-

3. noninverting amp :-



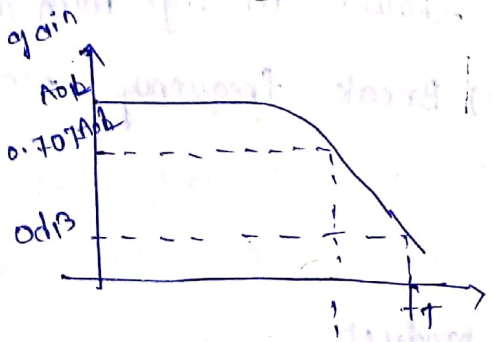

→ In a noninverting amplifier there is no phase difference the i/p and o/p voltages such an amp is shown in fig.

→ The inverting i/p terminal is grounded the signal $v_{i2}$ is applied at the noninverting terminal.

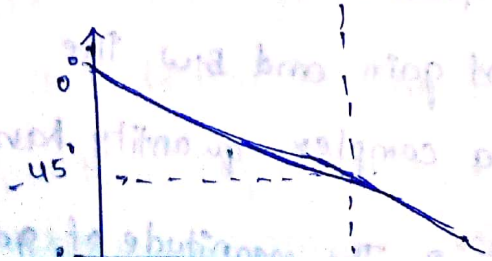
i.e $v_{i2} = 0$.

→ The +ve sine of o/p voltage implies that there is no phase inversion b/w o/p voltage and i/p voltage.

Frequency Response of op-amp :-




magnitude plot




phase plot

→ The open loop voltage gain of an op-amp ($A_{OL}$) is the ratio of the o/p voltage to the differential i/p voltage

i.e,

$$A_{OL} = \frac{V_o}{V_{id}}$$

→ The gain is purely a number being the ratio of 2 voltages however the gain can be usually expressed in decibals

$\therefore$ Voltage gain $= 20\log_{10}\left(\frac{V_o}{V_{id}}\right)$ dB.

→ The gain of an op-amp is a not a fixed magnitude But it is frequency dependent The gain changes with the change of frequency of the i/p signal.

→ This change of voltage gain with change of frequency is termed as frequency response of an op-amp

→ The Graphical representation of variations of gain with frequency is called frequency response curve (or) F.R. characteristic curve.

→ The frequency response curve as shown in fig. from the fig. Fo is the corner frequency (or) Break frequency.

→ The $\boxed{B.W = F_o - 0 = F_o \text{ Hz}}$

where Ft is the gain B.W product

→ It is defined as the product of gain and B.W The voltage gain of an op-amp is a complex quantity having both magnitude and phase at $f=0$ The magnitude

is max and the phase shift is 0°.

→ at F = Fo The corner frequency. The gain is 3dB less than the gain at F=0. and phase shift is −45°.

→ It is seen than the curve to beyond the corner frequency Fo the gain decreases almost linearly with w.r.to frequency

→ The slope of the linear part of the curve −20 dB for decade.

→ The Reduction of gain is with increase of signal frequency can be explain as follows

→ An op-amp mainly consisting of BJT (or) FET transist and these transistors having 3 junction transistor.

→ The impedence offered by a capacitance is given by

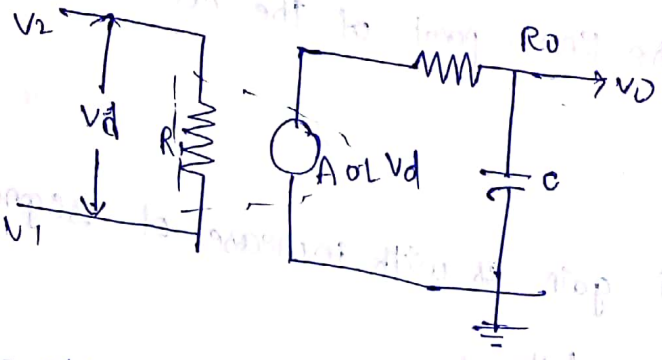
$$X_C = \frac{1}{2\pi f C t}$$

→ It is obvious that $X_C$ various inversily with frequency f at low frequencies $X_C$ is very large. and capacitor act as open ckt.

→ The higher frequencies the impedence of the capacitance becomes quiet small Due to the effect of capacitance the voltage gain reduces.

→ In addition to the internal capacitances is in the form junction capacitance, external - capacitance and also stray capacitance (or) parasitic capacitance.

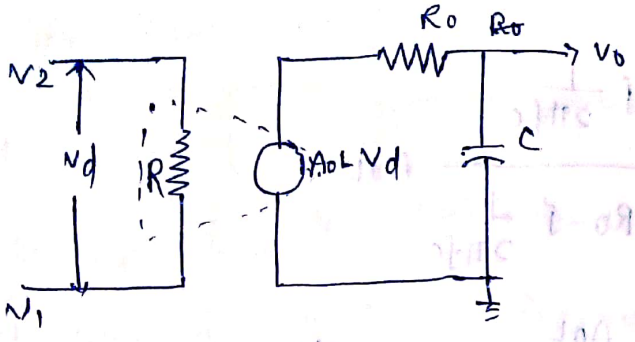
Because of these the op-amp gain decreases at higher frequencies is effect of capacitance is usually taken into account in the high frequency equalent ckt of op-amp by adding a capacitor in the o/p ckt as shown in the fig.

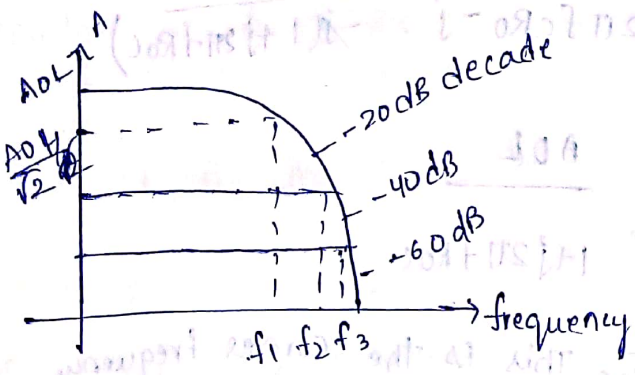



→ From the ckt we an use only 1 capacitor such that it has only one break frequency at the max phase shift is -90°. However, an op-amp can have several break frequencies such a case many capacitors at there break frequecies suppose we can take 2 Break frequencies two capacitor are available at 2 break freq max phase shift is -180°.

→ Three capacitors are available at 3 break freq the max phase shift is -270°.

## Expression for gain as a function frequency




→ consider the high frequency equivalent ckt of an op-amp with one break frequency as shown in figure.

→ from the ckt 'Ri' is the i/p resistance 'Ro' is the o/p resistance and 'C' is the capacitance.

→ Let AOL represents the open loop voltage gain at zero frequency. 'A' is the voltage gain at any frequency 'f'.

→ It is desired to obtain the expression for A interms of AOL and 'f'. From the ckt the o/p voltage

$$V_0 = \frac{-jX_c}{R_0 - jX_c} A_{OL} V_d$$

where $X_c = \frac{1}{2\pi fc}$

To sub $X_c$ in the above eqn

$$\frac{V_0}{} = \frac{-jX_c}{} A_{OL}$$

$$A = \frac{-jX_C}{R_0 - jX_C} A_{OL}$$

$$A = \frac{-j\frac{1}{2\pi fC}}{R_0 - j\frac{1}{2\pi fC}} A_{OL}$$

$$= \frac{-j A_{OL}}{2\pi f C R_0 - j} = \frac{-j A_{OL}}{-j(1 + j 2\pi f R_0 C)}$$

$$= \frac{A_{OL}}{1 + j 2\pi f R_0 C}$$

where $f_1 = \frac{1}{2\pi R_0 C}$ This is the corner frequency

$$A = \frac{A_{OL}}{1 + j(f/f_1)}$$

→ The magnitude of the gain $|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}$

phase $\phi = \tan^{-1}(f/f_1)$

→ let us obtain s domain equavalent of the gain A

i.e $A = \frac{A_{OL}}{1 + j(f/f_1)}$

$$= \frac{A_{OL}}{1 + j\left(\frac{2\pi f}{2\pi f_1}\right)} = \frac{A_{OL}}{1 + j\omega/\omega_1}$$

$$= \frac{A_{OL}}{j\omega + j\omega_1}$$

let $s = j\omega$. ∴ The explain expression can be

$$A = \frac{A_{OL}\omega_1}{s + \omega_1}$$

Since there is only one break frequency,

∴ The voltage transfer function has only one pole.

If the op-amp has several break frequencies then the voltage transfer function having many poles

→ let there are 3 break frequencies.

→ Denoted as $f_1, f_2, f_3$.

∴ The V.T.F $A = \frac{A_{OL}\, \omega_1 \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$

the corresponding frequency response as shown in fig.

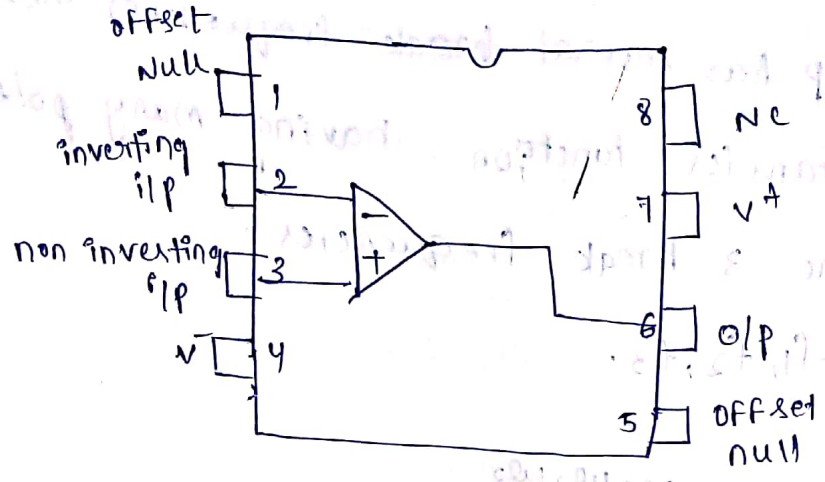
→ From the fig we can observed that frequency increases the voltage gain decreases blw $f_1$ and $f_2$.

the gain decreases at the rate of 20dB per decade blw $f_2$ and $f_3$.

→ The gain at the rate of 40dB per decade beyond $f_3$ at the rate of 60dB per decade.

→ At each break frequency causes a max phase shift of $-90^0$. blw the i/p and o/p voltages.

## IC 741 op-amp & its features:-




features:-

→ 1. The i/p impedence for IC741 op-amp is morethan 100kΩ.

2. The o/p impedence for IC741 op-amp is below 100Ω.

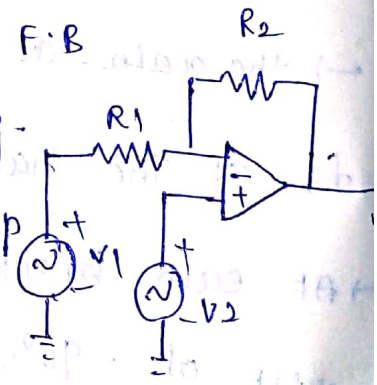
3. The frequency range of an op-amp is 0-1mHz.

4. The voltage gain of the IC741 op-amp is above (2,00,000)

5. The offset current and offset voltage of IC741 must be low.

## Stability of op-amp:-

→ consider an op-amp operating with -ve F.B path consists a resistor as shown in fig. let 'A' represents open-loop gain op-amp and 'ACL' represents closed loop gain.




we have

$$A_{CL} = \frac{A}{1+A\beta}$$

where $\beta$ is the F.B factor.

If a closed loop gain is said to be infinate gain then $1+A\beta=0$.

$$1-(-A\beta)=0$$
$$1-(-A\beta)=0.$$

$-A\beta$ represents the loop gain, where $A\beta$ is a complex quantity hence in order to satisfy the above conditions.

→ The magnitude must be unity.

i.e $|-A\beta| = 1$.

→ The phase is $\underline{|-A\beta} = 0$ (or) integer multiples $2\pi \times n$

→ From the ckt the F.B. loop is resistive in nature such that it doesnot produce any phase shift so the op-amp functioning as inverting amplifies then at low frequency their a phase shift of 180° b/w i/p & o/p.

→ The higher frequencies each break frequency introduced max phase shift -90° in open loop gain of op-amp has 2 break frequency of total phase shift will be -180°.

→ The magnitude of $-A\beta$ becomes equal to unity the phase shift becomes 360° (or) 0°.

→ The result of closed loop gain tends to become infinite.

∴ instability may be setup condition $A_{CL} > A$.

→ At low frequencies their is no additional phase shift caused by open loop gain A. and hence $A\beta$ is positive. This makes $A_{CL} < A$. which results the operation is quit stable.

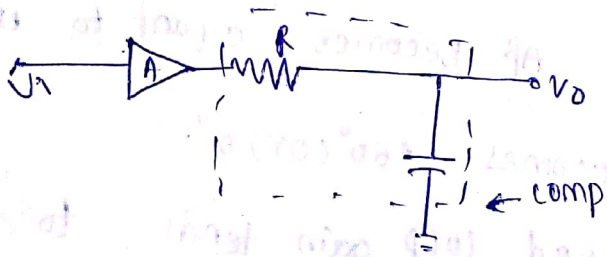
→ If a large B.w coupled with closed loop gain hau low is required in any practical applications suitable compensation technique must be adopted to prevent instability.

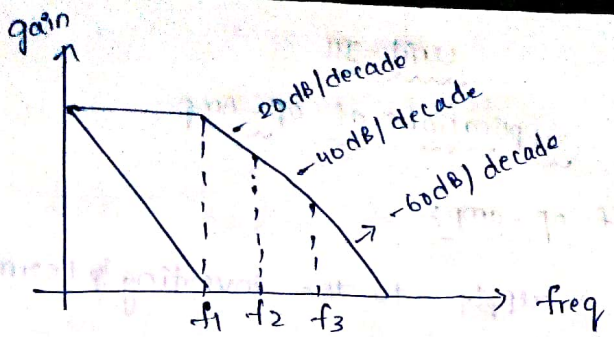
→ The following compensation techniques are generally used in order to gate the role of rate -20dB/decade over a ride range of frequencies.

1. Dominate pole compensating technique.
2. pole-zero " "

Dominate pole comp tech:-

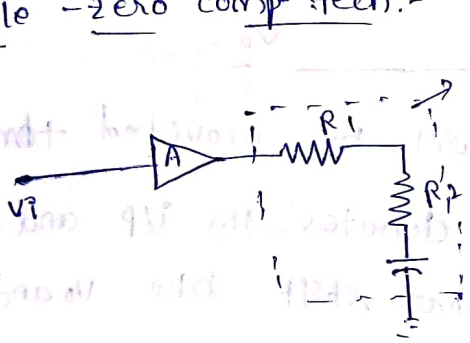
In this method the RC N/w is added inserie with op-amp as shown in fig.

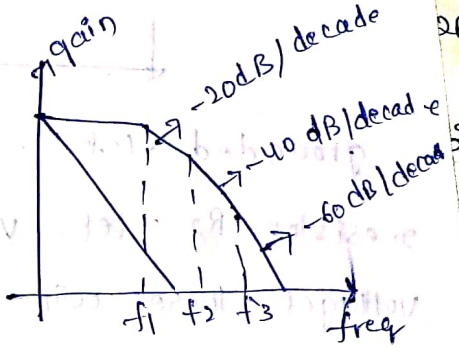





By using this technique to get required stability but the open loop B.w decrease.

Pole -zero comp tech:-




In this method of compensation the pole a zero added to the T.F by means of nlw as shown fig

→ Resistor $R_1$ is in series with the op-amp o/p terminal in the N/w $R_2C_2$ is connected across the o/p this tech increases the open loop B.w by making -20 dB/decade. slope line passes through odB line at the corner frequency $f_2$ instead of $f_1$.

→ By comparing above two tech it is seen that their is an increase of open loop B.w. equals to $f_2 - f_1$ by adopting the pole zero compensating tech instead of dominated pole compensating technique.