05/7/18

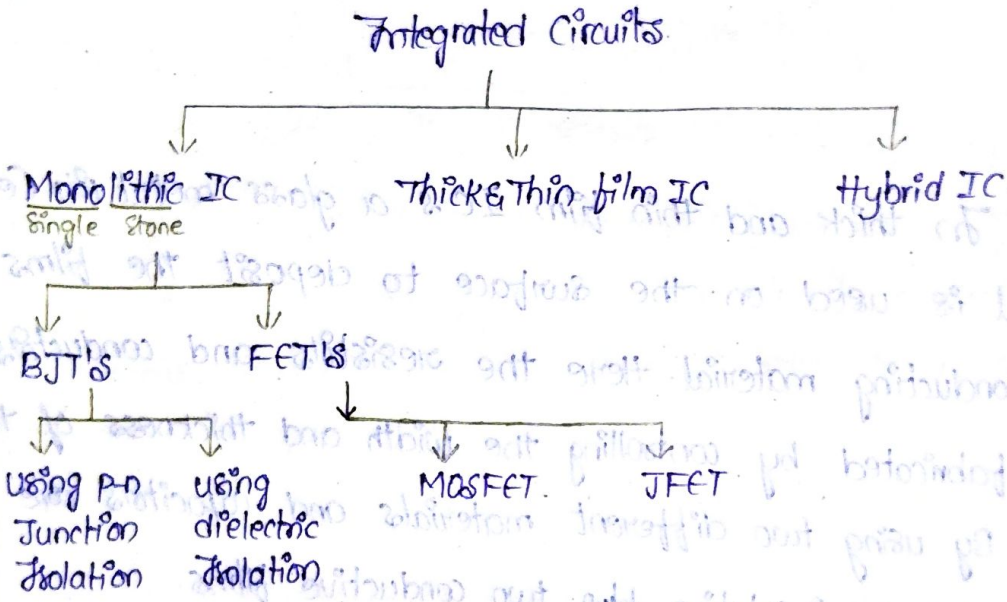
2. Integrated Circuit Technology and Operational Amplifiers

(21)

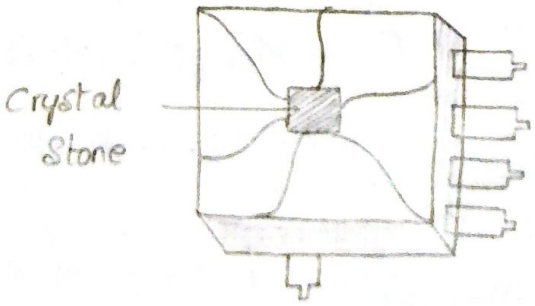
Def. of IC :-

Integrated circuit is defined as "a circuit which is fabricated (design) with both active components and passive components" such ckt is called as Integrated Circuit

Classification of IC's :-



Monolithic IC's :-



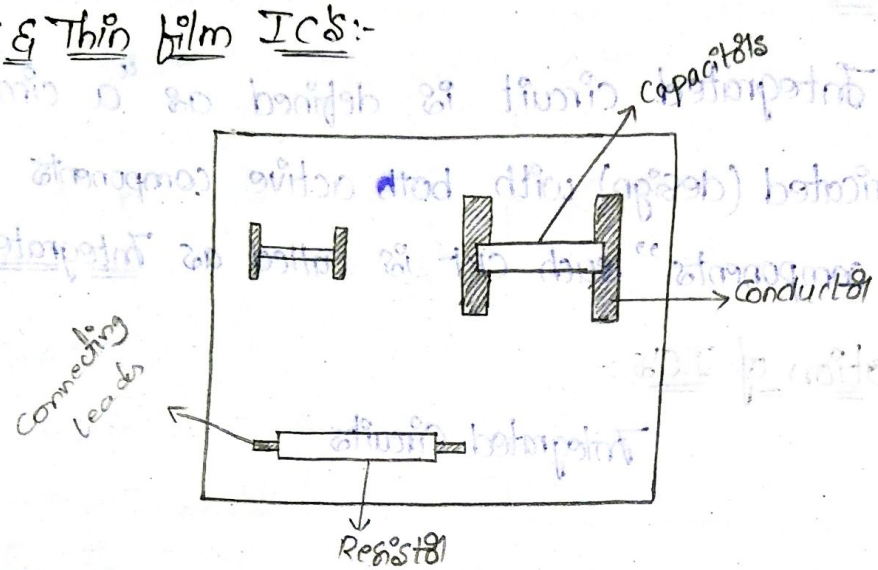
Monolithic IC's stands for all the active and passive components interconnected (or) integrated on a single crystal metal, the word of monolithic is a Greek word. It means that single stone i.e;

Mono - single

Lithic - Stone

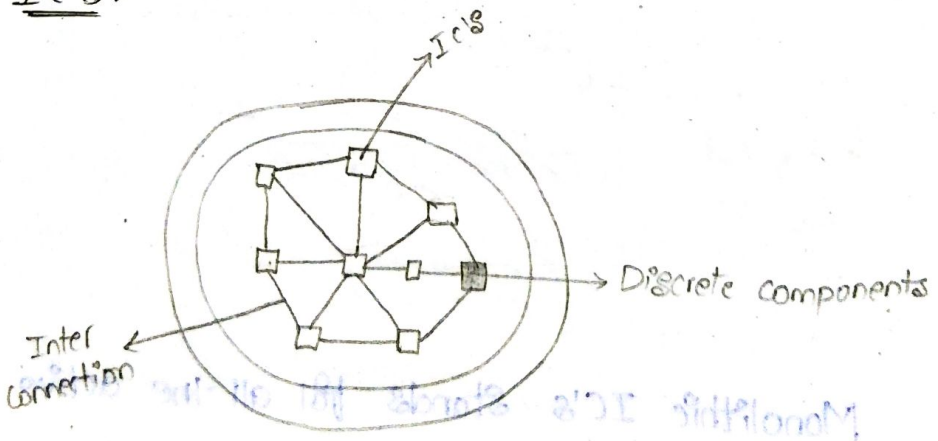
Monolithic IC's are preferred for the application in which the identical circuits are required in large number.

Thick & Thin film IC's:-



In thick and thin film IC's a glass metal (or) Ceramic metal is used on the surface to deposit the films of conducting material. Here the resistors and conductors are fabricated by controlling the width and thickness of the film. By using two different materials and capacitors are fabricated by insulating b/w two conductive films.

Hybrid IC's:-



Hybrid (or) Multi chip IC's are constructed by interconnecting a no. of individual chips (or) IC's. The active components are diffused and passive components are also diffused on a single chip. The connection b/w chips are

provided by wiring (or) metalised patterns.

The Hybrid technology gives better performance than Monolithic IC's.

6/4/18

IC chip size and levels of integration:-

The integrated circuit was introduced initially in 1947 by professor Bardeen and Brattain with the members of research at well laboratories invented by using first Germanium transistor.

Later in 1951 the BJT's and JFET's came into the market immediately in 1954 silicon transistor takes place of Ge in BJT's. Finally in 1958 professor Jack Kilby of texas instument invented the first Integrated circuit depending upon no. of active devices there are different levels of integrations.

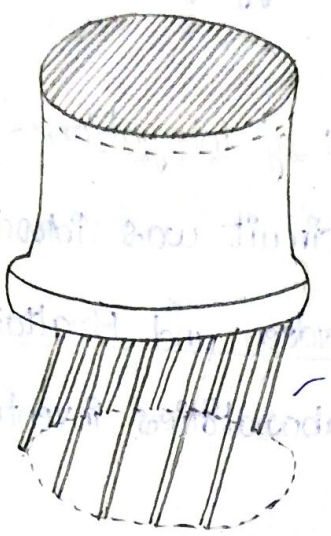
S.NO	Level of integration	Active devices per chip
1.	Small Scale integration (SSI)	< 100
2.	Medium Scale Integration (MSI)	100 - 10,000
3.	Large Scale Integration (LSI)	10,000 - 1,00,000
4.	Very Large Scale Integration (VLSI)	> 1,00,000
5.	Ultra Large Scale Integration (ULSI)	over Million

IC Packages:-

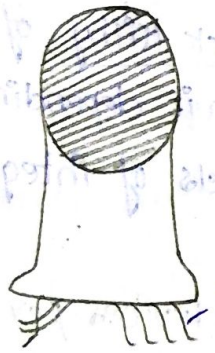
There are three types of packages available in market.

1. Metal Can (T_0) Package
2. Dual In Line package (DIP).
3. Flat pack package

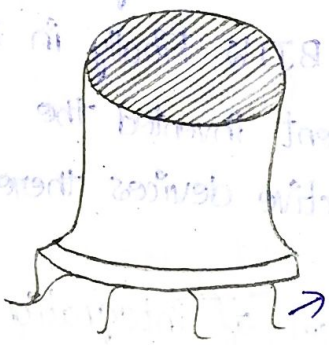
(1) Metal Can (To) Package :-



(a) To-5 style package (6, 8, 10 & 12 levels)



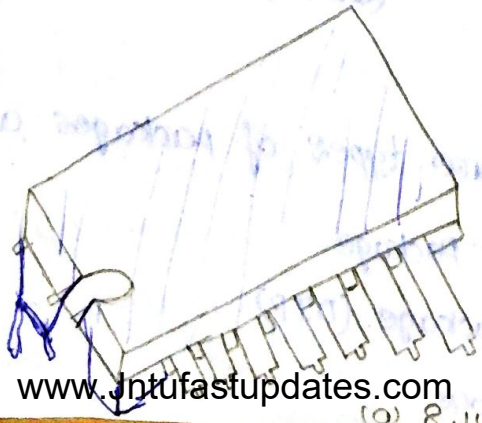
(b) To-5 style package 8-level

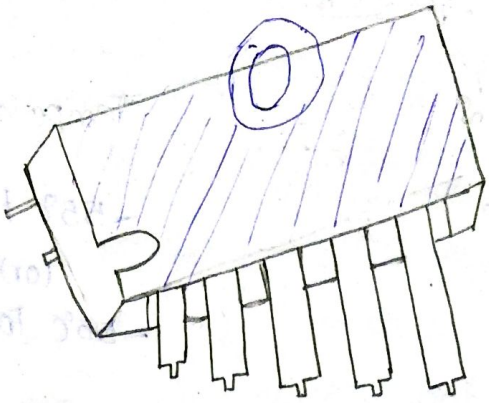


(c) To-5 style package 12-lead

The metal can packages available with 3, 5, 8, 10, 12 pins. The metal sealing plate is at the bottom over which the IC is bonded. This type of packages are well suited for power amplifiers in which the heat dissipation is important. So these packages are also called as Transistor Packages.

(2) Dual In line Package (DIP) :-



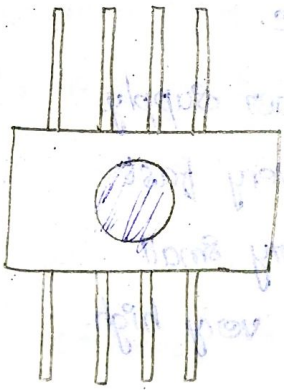


(b) 14,16 pin lead version

The dual in line packages are available in market with 8,12,14,16,20---- pins. In this type of chip which is mounted in side a plastic (or) ceramic metal. It is easy to handle, it can be placed easily and most widely used. The dual in line packages is popular for commercial applications.

In this 8-PIN dual in line package is called Mini-DIP.

(3) Flat Pack Package:-



(c) ceramic Flat package

Flat pack packages available in market with 8,10,14,16 pins. In this type of chip, the chip is enclosed in a rectangular ceramic cases. For the circuits where the space is critical the flat pack package gives a compatable package.

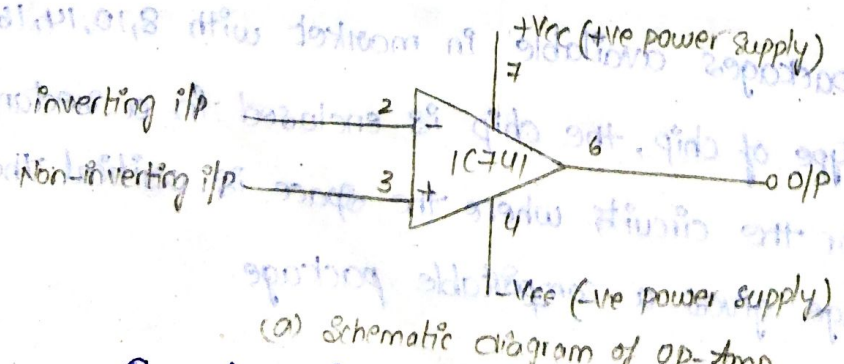
Temperature ranges of IC's:-

S.No	Application of IC's	Temperature Range
1.	Military purpose	-55°C to +125°C (or) -55°C to +85°C.
2.	Industry purpose.	-20°C to +85°C (or) -40°C to +85°C.
3.	Commercial purpose	0°C to 75°C. (or) 0°C to 70°C.

Advantages of IC's:-

1. Low cost.
2. Required low power consumption.
3. It is highly reliable.
4. It requires low power supply.
5. The speed of IC is very fast.
6. The size of IC is very small.
7. Life time of IC's is very high.

* Operational Amplifier:-



(a) Schematic diagram of op-amp

Op-Amp is defined as an amplifier which perfforms multiple operations such an amplifier is called Op-Amp

From the schematic diagram of Op-Amp

(i) The second pin is the inverting i/p terminal (−)

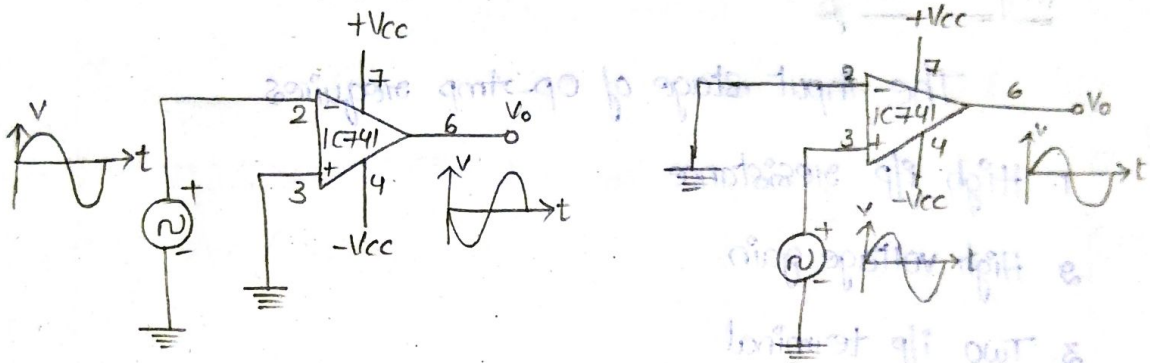
(ii) The third pin is the non-inverting i/p terminal (+).

(iii) The fourth pin is the -ve power supply (-Vee).

(iv) The seventh pin is the +ve power supply (+Vcc).

(v) The sixth pin is the o/p terminal.

Operation of Op-Amp:-



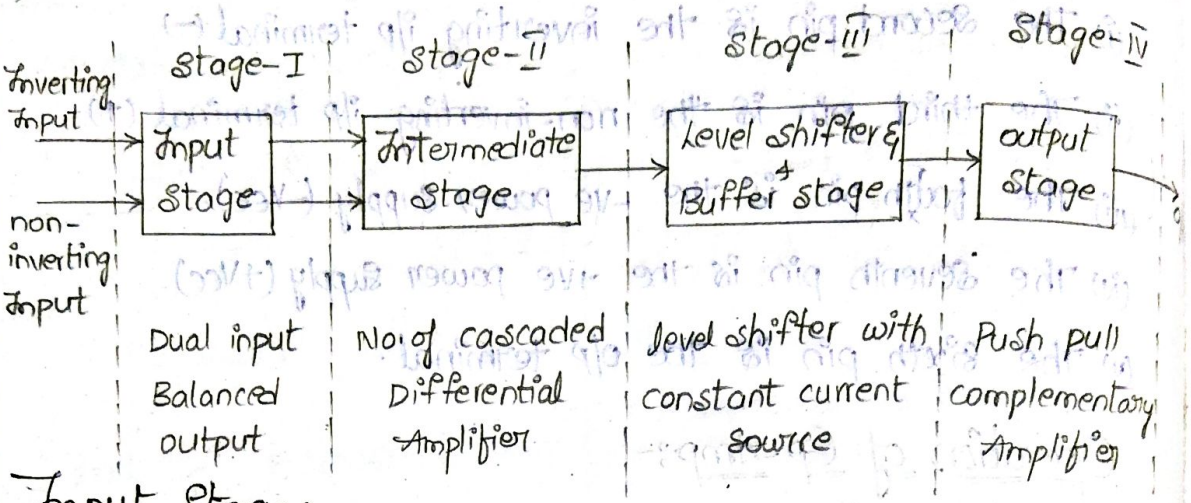
(a) Inverting Operation (b) Non-Inverting operation

From the operational Amplifier, when the i/p is applied to the inverting terminal respective other terminal (non-inverting) make it as grounded. Such operation is called as Inverting Operation.

Similarly when the input is applied for non-inverting terminal and respective other terminal make it as grounded. Such operation is called as Non-Inverting.

From the above circuits, the inverting output is 180° out of phase with its non-inverting terminal. That means the o/p response is exactly opposite phase response. While for non-inverting operation same output response is produced.

* Block diagram of Op-Amp :-

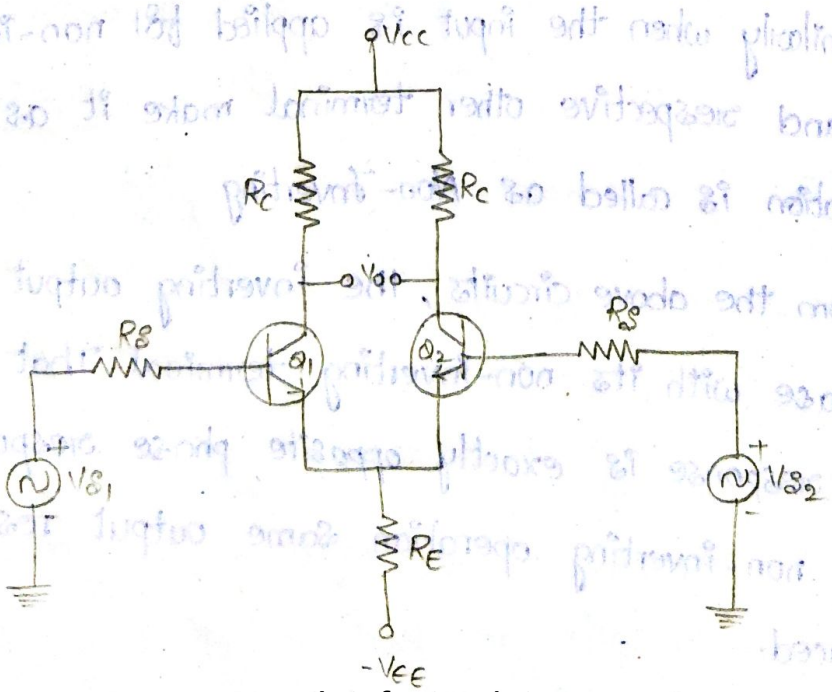


Input Stage :-

The input stage of Op-Amp requires

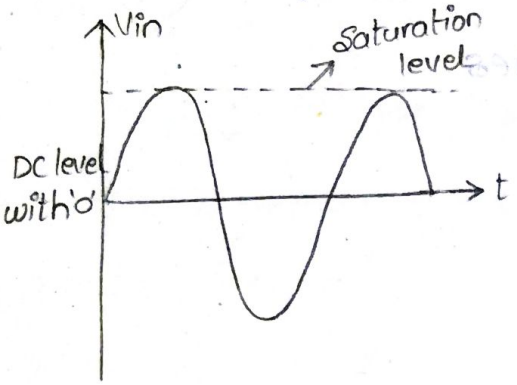
1. High i/p resistance
2. High voltage gain.
3. Two i/p terminal.
4. Low off-set voltage.
5. Low off-set current.
6. Low i/p bias current.
7. High CMRR.

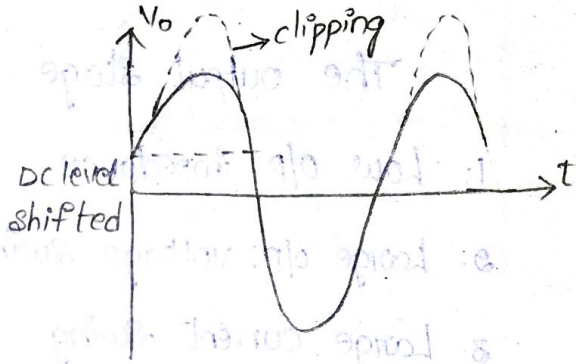
All this above requirements can provides only by the DIBO. Hence DIBO is used as i/p state for an op-Amp



Intermediate Stage:-

The o/p of the i/p stage devices is the intermediate stage which is an another type of differential amplifier with D.I.U.B.O i.e; single ended o/p. The overall gain requirement of an op-Amp is very high, the i/p stage is alone. Cannot provide such a high gain. The main function of intermediate stage is to provided additional gain requirement.



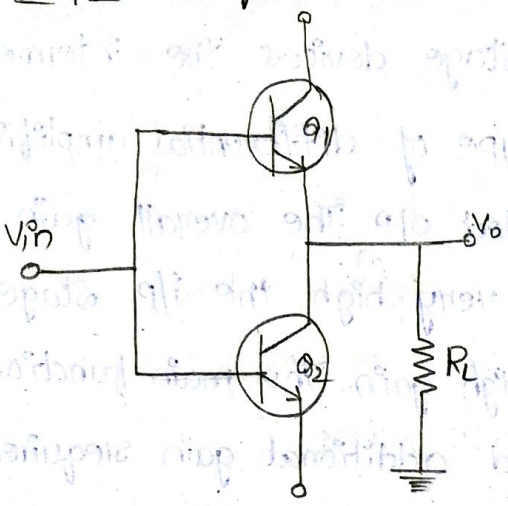


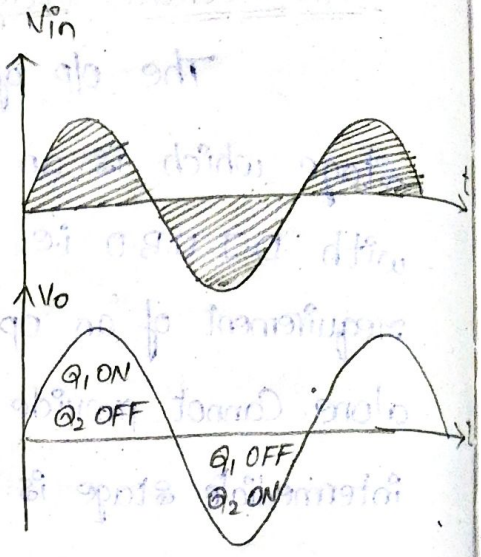
Level Shifter and Buffer

All the stages are directly connected to each other as the op-amp DC signal also the caupling capacitors are not used cascaded the stages. Hence the DC level of the previous stage gets applied as the i/p for the next stage. Hence stage by stage DC level increases well above the grounded as in the fig (b). Such DC voltage may drive the transistor into situation this may further causes a distortion in the o/p due to the clipping and maximum limitation of o/p swing.

Before the o/p stage, it is necessary to bring down the DC level to zero w.r.t. ground. This is achieved by level translator and the buffer is usually an emitter follower whose input impedance is very high.

Output Stage :-





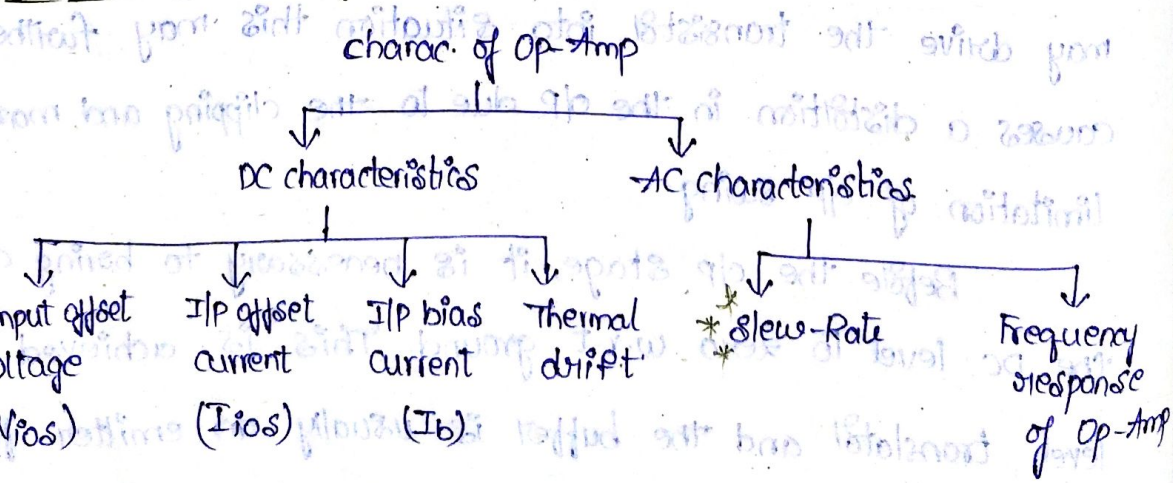
The output stage requires

1. Low o/p impedance.
2. Large o/p voltage swing.
3. Large current swing.
4. Short circuit protection.
5. Heat sinking capability.

All the above requirements satisfied by the push-pull complementary amplifier.

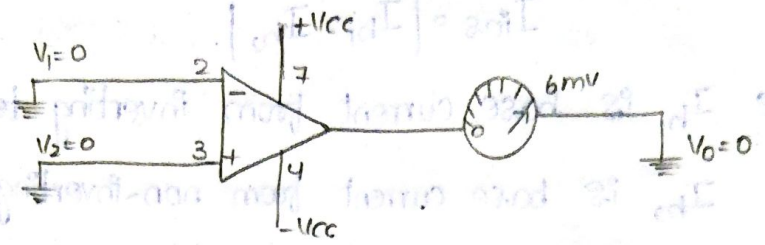
Hence the o/p stage is used this amplifier generally class-B (or) class-AB amplifier.

Characteristics of Op-Amp :-

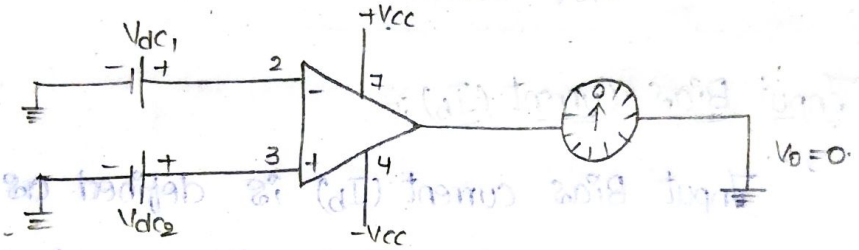


① DC characteristics :-

(i) Input offset voltage (V_{ios}) :-



(a) Inputs applied as offset voltage



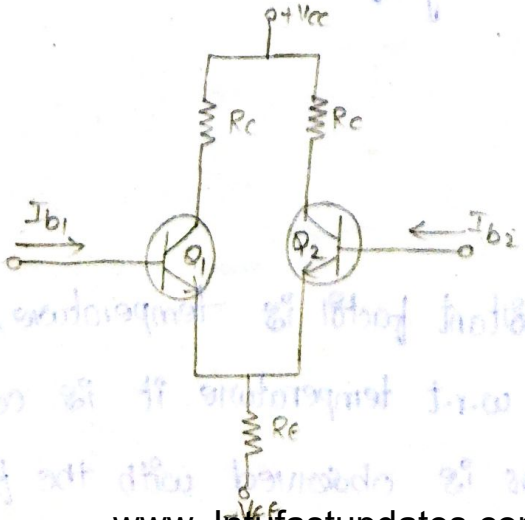
(b) offset voltage to "zero"

→ The differential voltage that must be applied b/w two i/p terminals of an Op-Amp. to make the o/p voltage "zero" is called as Input offset voltage (V_{ios}) i.e;

$$V_{ios} = |V_{dc_1} - V_{dc_2}|.$$

* For practical IC741 op-Amp
$V_{ios} = 6mV.$

(ii) Input offset Current (I_{ios}) :-



Input offset Current is defined as the difference b/w the both base currents of inverting and non-inverting terminals i.e;

$$I_{ios} = |I_{b_1} - I_{b_2}|.$$

where I_{b_1} is base current from inverting terminal.

I_{b_2} is base current from non-inverting terminal.

* For practical IC741 op-Amp

$I_{ios} = 200nA.$

(iii) Input Bias Current (I_b) :-

Input Bias current (I_b) is defined as the average values of both currents flowing from the bases of the transistors of Q_1 and Q_2 i.e;

$$I_b = \frac{I_{b_1} + I_{b_2}}{2}.$$

* For practical IC741 op-Amp

$I_b = 500nA$

(iv) Thermal Drift :-

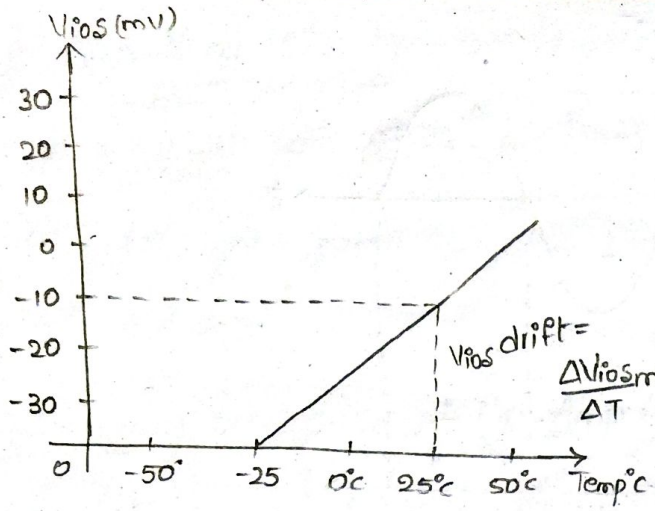
The i/p offset voltage (V_{ios}), Input offset current (I_{ios}) and i/p Bias current (I_b) are not constant. These parameters change with the following factors.

(1) Temperature.

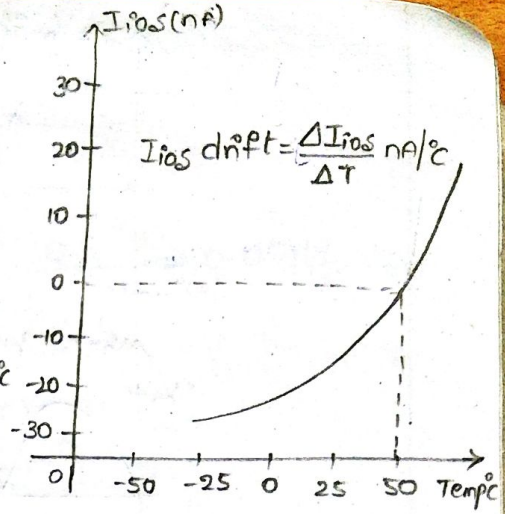
(2) Supply voltage.

(3) Time.

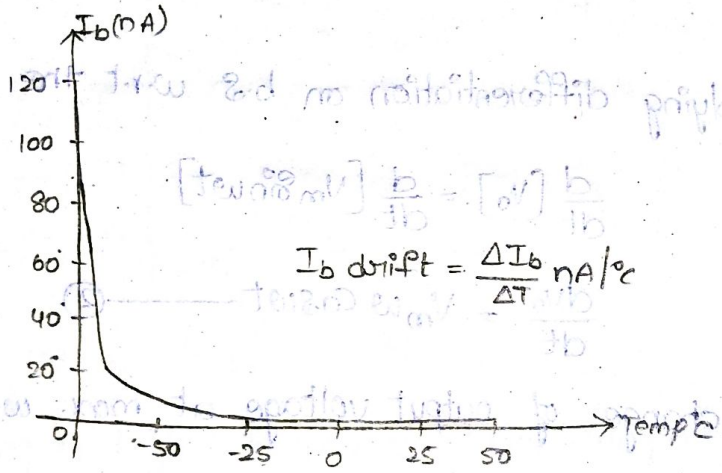
The most important factor is temperature, if V_{ios}, I_{ios} and I_b is varied w.r.t temperature it is called as the Drift. The changes is observed with the following figures.



(a) Effect of Temp. with Vios



(b) Effect of Temp. with Ios



(c) Effect of Temp. with Ib.

12/7/18

② AC characteristics :-

(i) Slew-Rate :-

Slew-Rate is defined as the max. rate of change of o/p voltage w.r.t the time is called as Slew-Rate.

i.e;

$$\text{Slew-Rate} = \left.\frac{dV_o}{dt}\right|_{max}$$

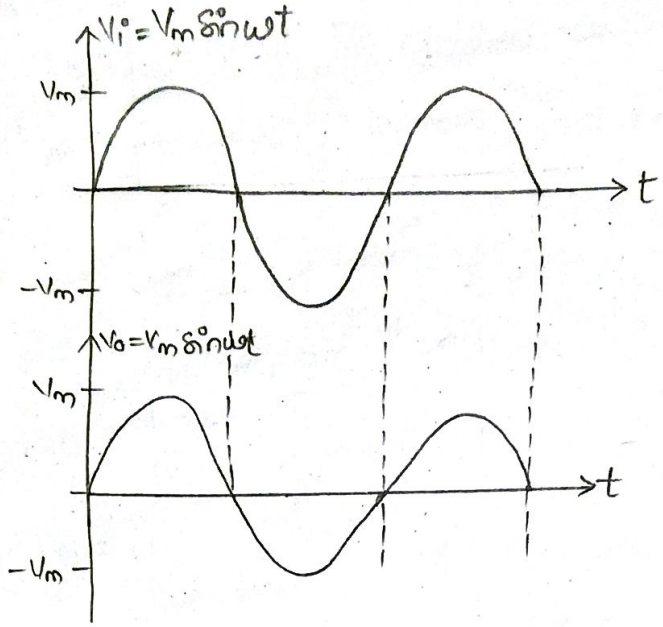
It is expressed in volts/μs.

Equation for Slew-Rate :-

Let us consider the i/p voltage

$$V_i = V_m \sin \omega t$$

Hy the output voltage is also $V_o = V_m \sin \omega t$ ——— ①



Applying differentiation on b.s w.r.t the time for eq ①

$$\frac{d}{dt}[V_o] = \frac{d}{dt}[V_m \sin \omega t]$$

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t \quad \text{——— ②}$$

The change of output voltage at max. w.r.t time at a unity gain of $\cos \omega t = 1$

$$\therefore \left.\frac{dV_o}{dt}\right|_{max} = V_m \cdot \omega (1)$$

i.e; $$\boxed{\text{Slew-Rate} = \left.\frac{dV_o}{dt}\right|_{max} = V_m \cdot 2\pi f_{max}} \quad \because [\omega = 2\pi f] \quad \text{——— ③}$$

From eq ③

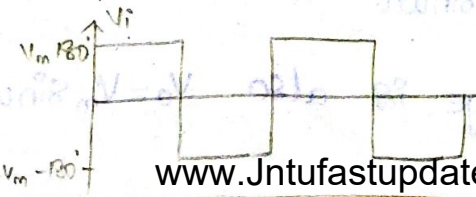
$$\boxed{f_{max} = \frac{S\text{-}R}{V_m \cdot 2\pi}} \quad \text{——— ④}$$

The eq ④ is called as full power Bandwidth.

Problem:-

① An Op-Amp operates as a unity gain buffer with $3V_{p-p}$ square wave input. If the Op-Amp is ideal with slew-Rate is $0.5 V/\mu s$ Then find full power Bandwidth?

Sol:-



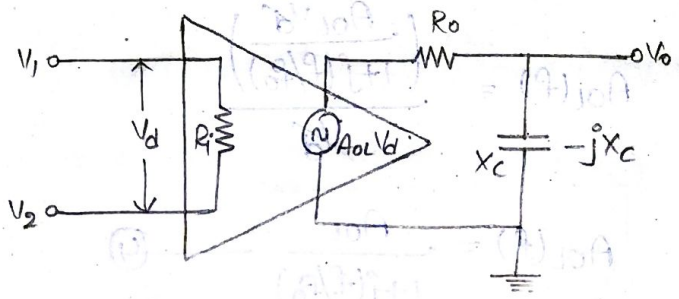
Given Slew-Rate is = 0.5V/μsec

Then full power Bandwidth is $f_{max} = \frac{S.R}{V_m \cdot 2\pi}$

$= \frac{0.5}{1.5 \times 2\pi} = 0.05Hz$

(ii) Frequency response of Op-Amp (or)

High Frequency Model Analysis:-



(a) High frequency Model

By using a High frequency Model analysis, from above fig. to obtain the frequency response of the elements. Let us consider $-jXc$ (or) $\frac{1}{jXc}$ is the capacitive reactance of the capacitor. Then according to the voltage divider rule we can write the o/p voltage from the above fig. is

$$V_o = \left[-jX_c / R_o - jX_c\right] A_{OL} V_d \quad \text{——} (1)$$

Here W.K.T $-j = \frac{1}{j}$ and $X_c = \frac{1}{2\pi f c}$.

$$V_o = \left[\frac{\frac{1}{j2\pi fc}}{R_o + \frac{1}{j2\pi fc}}\right] A_{OL} V_d$$

$$\boxed{V_o = \frac{A_{OL} V_d}{1 + j2\pi f R_o C}}$$

From the above expression we can write

$$V_o = \frac{A_{OL} V_d}{1 + j\left(\frac{f}{f_o}\right)} \quad \text{where } f_o = \frac{1}{2\pi R_o C} \qquad \text{---- (2)}$$

W.K.T the open loop gain of frequency function is expressed as

$$A_{OL}(f) = \frac{V_o}{V_d} \qquad \text{---- (3)}$$

Sub eq (2) in eq (3)

$$A_{OL}(f) = \frac{\left(\frac{A_{OL} V_d}{1 + j(f/f_o)}\right)}{V_d}$$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j(f/f_o)} \qquad \text{---- (4)}$$

eq (4) states that $A_{OL}(f)$ is the gain as a function of frequency 'f' is the operating frequency. From eq (4) we can write the magnitude response and phase response.

i.e; Magnitude response is

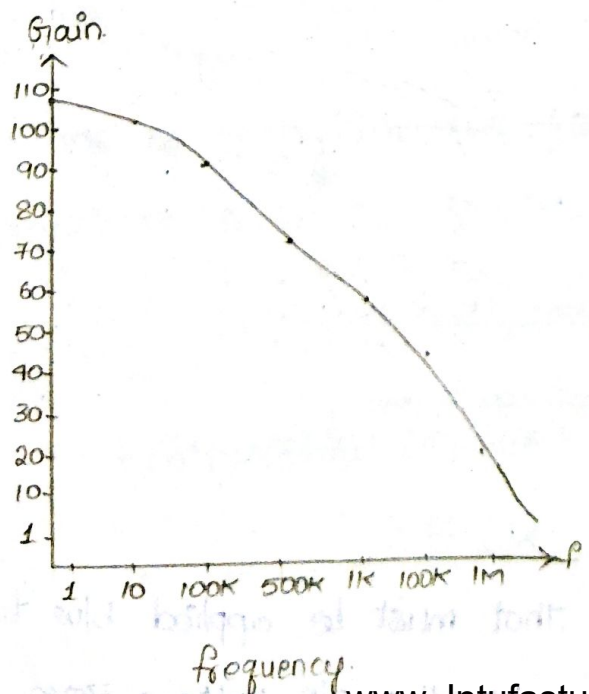
$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}} \qquad \text{---- (5)}$$

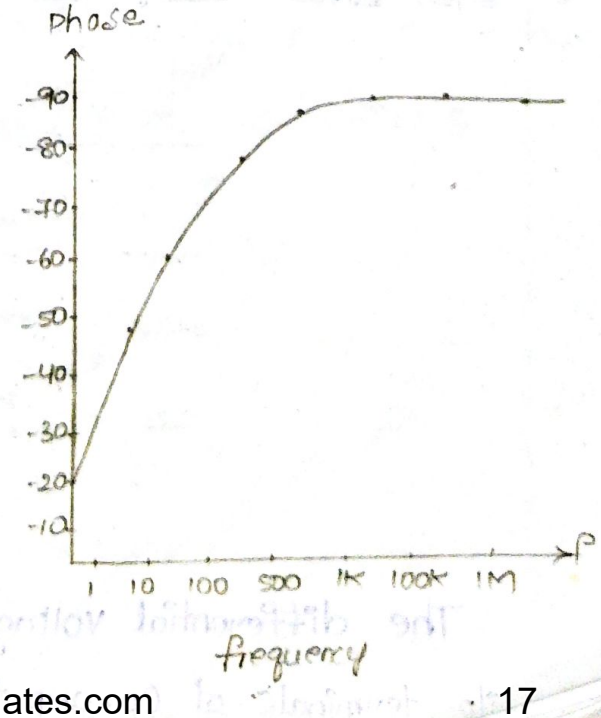
and the phase response is

$$\angle A_{OL}(f) = -\tan^{-1}\left(\frac{f}{f_o}\right) \qquad \text{---- (6)}$$

For an IC op-Amp 741 consider the cut-off frequency f_o as 5Hz and open loop gain is 2 lakhs. Then the frequency response is obtained as follows.

	I/P frequency (f)	$A_{OL}(f) = 20\log\left[\frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_0}\right)^2}}\right]$	$\angle A_{OL}(f) = -\tan^{-1}\left(\frac{f}{f_0}\right)$
1.	0HZ	$A_{OL}(f) = 20\log \frac{2,00,000}{\sqrt{1+\left(\frac{0}{5}\right)^2}}$ $= 106.02$	$\angle A_{OL}(f) = \tan^{-1} \frac{2,00,000}{(0/5)}$ $= 0$
2.	5HZ	$A_{OL}(f) = 20\log \frac{2,00,000}{\sqrt{1+\left(\frac{5}{5}\right)^2}}$ $= 103.01$	$\angle A_{OL}(f) = \tan^{-1}(5/5)$ $= -45°$
3.	10HZ	$A_{OL}(f) = 20\log \frac{2lakhs}{\sqrt{1+\left(\frac{10}{5}\right)^2}}$ $= 99.03$	$\angle A_{OL}(f) = \tan^{-1}(10/5)$ $= 63.43$
4.	100HZ	$A_{OL}(f) = 20\log \frac{2,00,000}{\sqrt{1+\left(\frac{100}{5}\right)^2}}$ $= 79.9$	-87.1
5.	500HZ	66.0	-89.4
6.	1K	59.9	-89.71
7.	100KHZ	9.99	-89.99
8.	1MHZ	1	-89.99

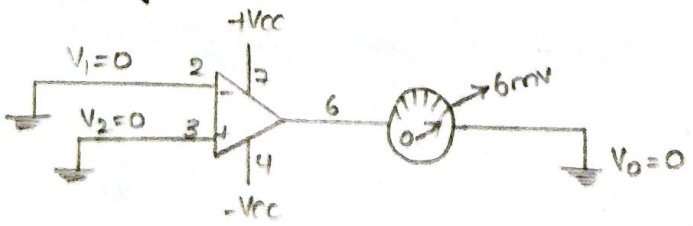




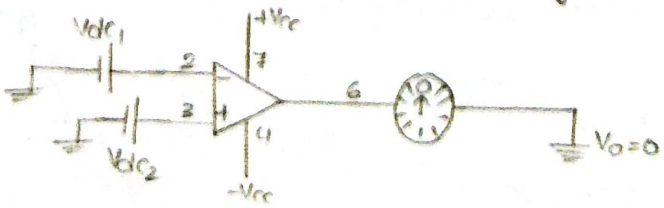
Parameters and characteristics of Op-Amp :-

1. Input offset voltage (V_{ios})
2. Input offset current (I_{ios})
3. Input Bias current (I_b)
4. Differential input resistance (R_i)
5. Input Capacitance (C_i)
6. Open loop gain (A_{OL})
7. Common Mode Rejection Ratio (CMRR) (or) (ρ).
8. Output Voltage Swing.
9. Output Resistance (R_o)
10. Input Voltage Range.
11. Power Supply Rejection Ratio (PSRR)
12. Power Consumption.
13. Slew Rate.
14. Gain Bandwidth Product
15. Output offset Voltage.
16. Average Temperature Coefficient (or) Thermal drift
17. Offset voltage Adjustment Range (or) Offset Null.

(1) Input offset Voltage (V_{ios}) :-



(a) inputs applied as offset voltage



(b) offset voltage to zero

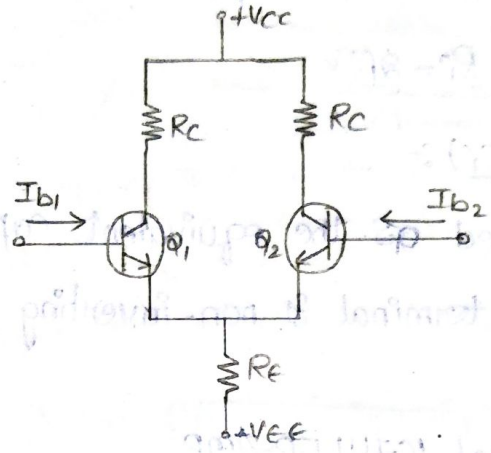
The differential voltage that must be applied b/w two terminals of Op-amp to make the o/p voltage zero is

called as input offset voltage (V_{ios}). i.e;

$$V_{ios} = |V_{dc_1} - V_{dc_2}|.$$

> for practical, IC741 op-Amp
> $V_{ios} = 6mV$

(2) Input offset Current (I_{ios}):-



Input offset current is defined as the difference b/w the both base currents of inverting and non-inverting terminals ie;

$$I_{ios} = |I_{b_1} - I_{b_2}|.$$

where I_{b_1} is the base current from inverting terminal and I_{b_2} is the base current from non-inverting terminal.

> For practical IC741 op-Amp
> $I_{ios} = 200nA$

(3) Input Bias Current (I_b):-

Input Bias Current (I_b) is defined as the average values of both currents flowing from the bases of transistors Q_1 and Q_2. ie;

$$I_b = \frac{I_{b_1} + I_{b_2}}{2}$$

> F81 practical Op-Amp IC741
> $I_b = 500nA$

(4) Differential input resistance: (R_i)

It is defined as the equivalent resistance measured either at inverting terminal & non-inverting terminal with the other terminal is grounded.

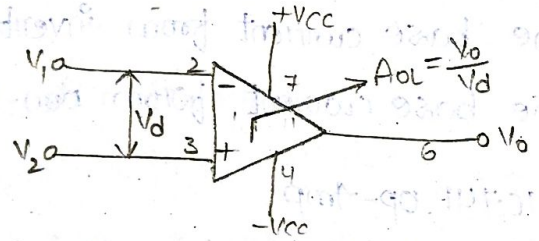
For practical IC741 Op-Amp
$R_i = 2M\Omega$

(5) Input Capacitance (C_i):-

It is defined as the equivalent capacitance measured either at inverting terminal & non-inverting terminal with the other

For practical IC741 Op-Amp
$C_i = 1.4\ PF$

(6) Open loop gain (A_{OL}):-



Open loop gain (A_{OL}) is defined as the ratio of o/p voltage V_o to differential voltage V_d

$$i.e;\ A_{OL} = \frac{V_o}{V_d}$$

For practical IC 741 Op-Amp
$A_{OL} = 2 \times 10^5$
$= 2,00,000.$

(7) CMRR (ρ):-

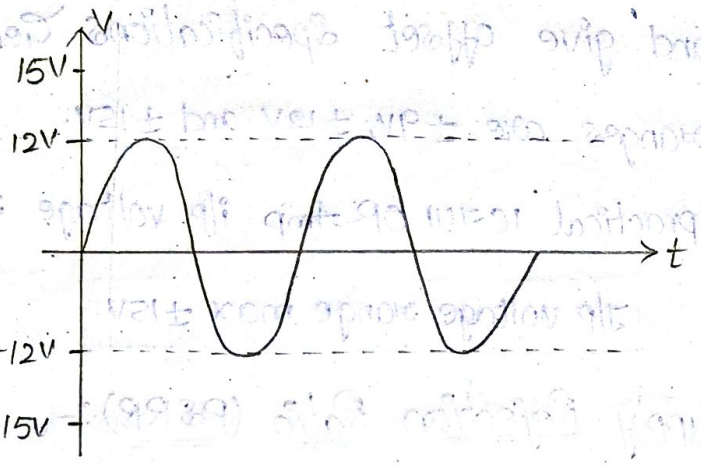
It is defined as the ratio of differential mode gain (A_d) to the common mode gain (A_c).

$$CMRR = \frac{A_d}{A_c}$$

For practical IC741 op-Amp

CMRR = 90dB.

(8) Output Voltage Swing :-

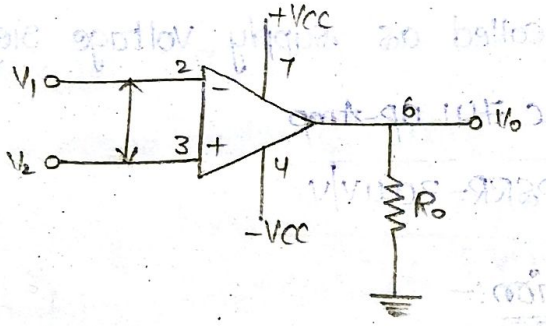


The o/p of the Op-Amp is limited i.e; the o/p get decided by the supply voltage. It never exceeds +Vcc and -Vcc. Such o/p voltage is called as Output Voltage Swing.

For practical IC741 Op-Amp o/p voltage swing is

o/p voltage Swing = ±15V.

(9) Output Resistance (R_o) :-



Output resistance R_o is defined as the equivalent resistance measured btw o/p terminal and ground.

For practical IC741 Op-Amp

$R_o = 75\Omega$

(10) Input Voltage Range:-

It is the range of common mode voltage which can be applied for an Op-Amp where the Op-Amp functions properly and give offset specifications. Generally the i/p voltage ranges are ±9V, ±12V and ±15V.

For practical IC741 OP-Amp i/p voltage range is

i/p voltage range max ±15V

(11) Power Supply Rejection Ratio (PSRR):-

Power Supply Rejection Ratio is defined as the ratio of change of input offset voltage due to the change in supply voltage. It is measured in μv/v (or) mv/v. mathematically it is expressed as

$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{cc}}\Big|_{V_{ee}\ constant}$$

$$= \frac{\Delta V_{ios}}{\Delta V_{ee}}\Big|_{V_{cc}\ constant}$$

PSRR is also called as supply voltage rejection ratio

for practical IC 741 op-Amp

PSRR = 30μv/v.

(12) Power Consumption:-

It is defined as the amount of the power to be consumed by the op-Amp with zero input voltage.

for practical IC741 op-Amp

P_c = 85mV

(13) Slew Rate:-

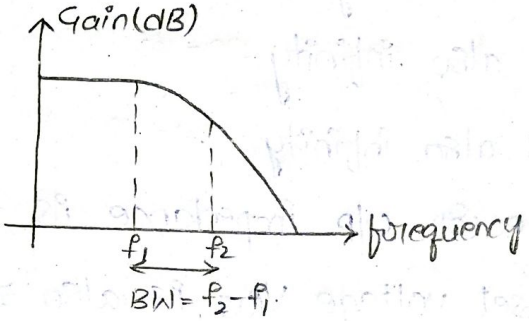
Slew Rate is defined as the rate of change of o/p age w.r.t time at max value. Units for slew rate is v/μsec

i.e; $SR = \left.\frac{dV_o}{dt}\right|_{max}$

For practical IC-741 op-Amp,

$$\boxed{SR = 0.5\ V/\mu sec}$$

(14) Gain Bandwidth Product :-



It is defined as the op-Amp whose voltage gain is unity. That Bandwidth is called as Gain Bandwidth. It is expressed in decibles.

For practical IC-741 op-Amp

$$\boxed{\text{Gain Bandwidth} = 1MHz}$$

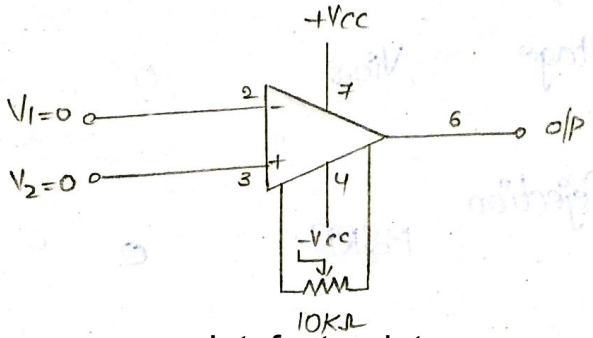
(15) Output offset Voltage :-

It is defined as the DC voltage present at o/p terminal when both inputs are grounded.

(16) Average temperature coefficient (or) Thermal drift :-

The average rate of change of i/p offset voltage with unity change in temperature is called as Average temperature coefficient of input offset voltage or drift

(17) Offset Voltage Adjustment Range :-



If an Op-Amp is said to be ideal it is satisfying the following conditions, the open loop gain is infinity

(1) $A_{OL} = \infty$

(2) Input impedance (or) input resistance is always infinity R_i (or) $Z_i = \infty$

(3) CMRR is also infinity. $CMRR = \infty$

(4) Slew rate is also infinity. $SR = \infty$

(5) Bandwidth is also infinity. $B.W = \infty$

(6) O/p resistance (or) O/p impedance is zero. R_o (or) $Z_o = \infty$

(7) The input offset voltage V_{ios} is also zero.

(8) Power Supply rejection ratio is zero.

1. Give the comparision between ideal OP-Amp characteristics Vs practical Op-Amp characteristics.

S.No	Characteristics	Symbol	Ideal Value	Practical Value
1.	Open loop gain	A_{OL}	∞	2×10^5
2.	Input impedance (or) Input resistance	Z_i (or) R_i	∞	2MΩ
3.	CMRR	ρ	∞	90dB.
4.	Slew Rate	SR	∞	0.5V/μsec.
5.	Bandwidth	BW	∞	1MHz
6.	Output Impedance (or) Output resistance	Z_o (or) R_o	0	75Ω
7.	Input offset voltage	V_{ios}	0	6mV.
8.	Power Supply Rejection Ratio	PSRR	0	30μV/V.

17/18 Explain the factors effecting in parameters of Op-Amp.

factors effecting parameters of Op-Amp

Supply voltage	frequency	Temperature
↓ Factors	↓ Factors	↓ Factors
(1) o/p voltage swing	(1) I/p resistance R_i	(1) Input offset current
(2) o/p voltage range	(2) o/p resistance R_o	(2) I/p Bias current
(3) power consumption	(3) CMRR	(3) Power Consumption
(4) I_{OS}	(4) o/p noise voltage	(4) Gain Bandwidth product
	(5) I/p noise voltage	

Output Noise Voltage:-

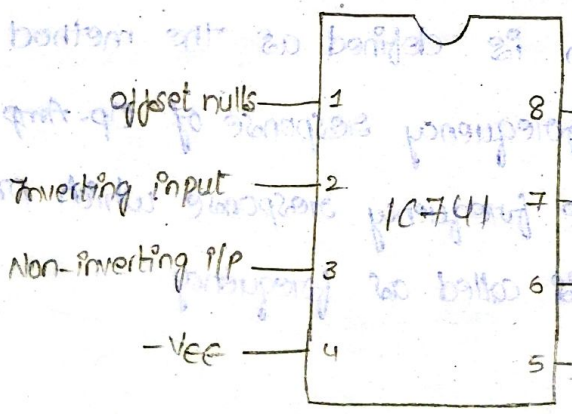
O/p Noise voltage is defined as the noise produced at the o/p voltage with the o/p terminal is grounded across th terminal such noise is called as Output Noise V

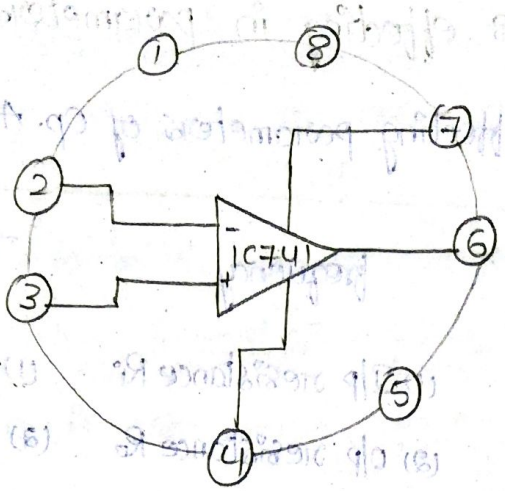
Input Noise Voltage:-

From the Op-Amp terminals if the noise is either inverting terminal (or) non-inverting terminal w.r.t to other terminal is grounded. Such noise is called as I/p noise voltage.

(Refer parameters of Op-Amp) ⇒ Remaining.

IC741 Op-Amp and its features:-





Features:-

(i) IC741 op-Amp is not required frequency compensation technique.

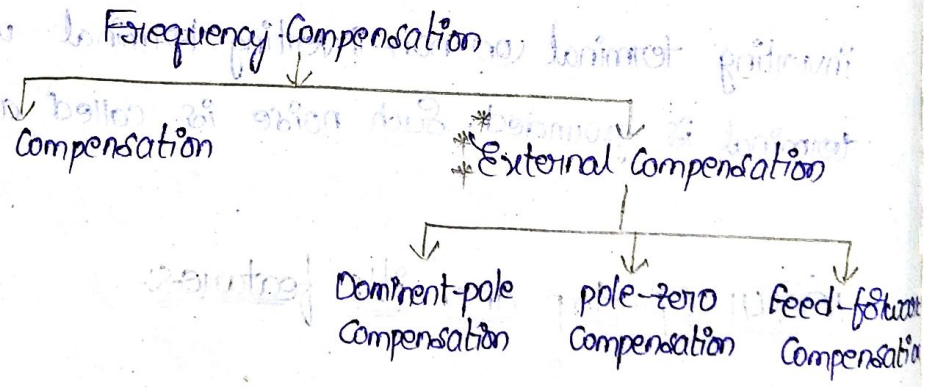
(ii) It requires short circuit protection.

(iii) It requires offset null in capacitance.

(iv) It requires large differential mode and common mode voltage range

(v) It doesn't require any Latch-up

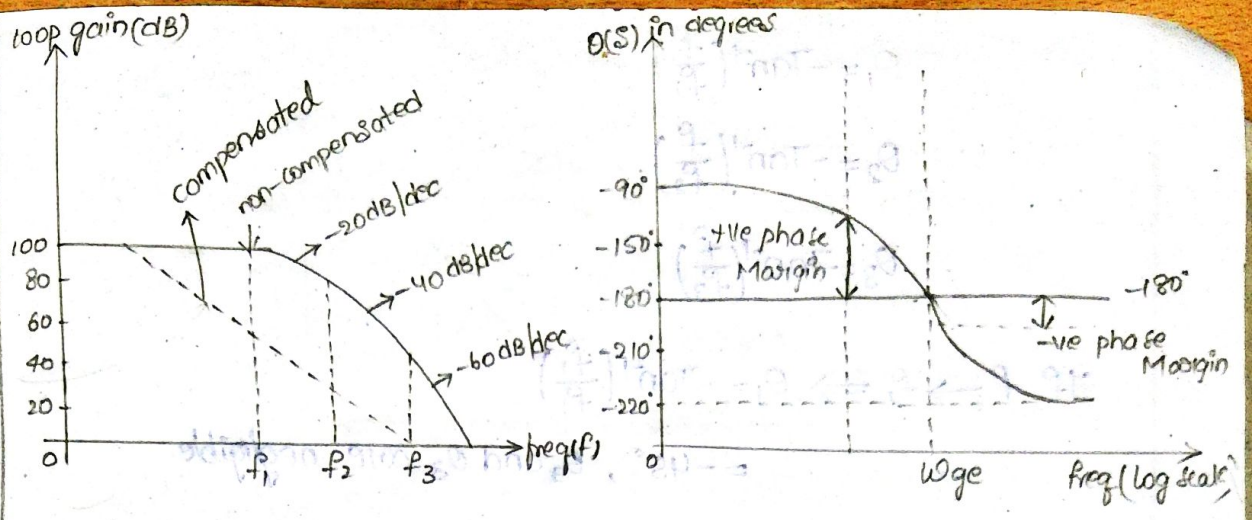
Frequency Compensation technique:-



Frequency compensation is defined as the method which modifying the loop gain frequency response of Op-Amp. It behaves like single brake frequency response which provides sufficient phase margin is called as frequency

Internal Compensation:-

The op-Amp ckt with a single brake frequency is not always stable. Consider the system with 3 brake frequencies (or)



corner frequencies. This is possible in practice due to the capacitive component produced by various no. of stages. Then the open loop dependent transfer function of such system can be expressed as

$$A_{OL}(f) = \frac{A_{OL}\ (at\ f=0)}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]} \quad \text{——— (1)}$$

where $0 < f_1 < f_2 < f_3$

In practice a transfer function of above eqn can be expressed in Laplace transform which is

$$A_{OL}(f) = \frac{A_{OL}}{(S+\omega_1)(S+\omega_2)(S+\omega_3)} \quad \text{——— (2)}$$

where A_{OL} = loop gain at zero frequency

$\omega_1, \omega_2, \omega_3$ = corner frequencies such that $0 < \omega_1 < \omega_2 < \omega_3$.

Now from eq (1) the phase shift introduced such a loop gain is

$$\phi(t) = -\tan^{-1}\left(\frac{f}{f_1}\right) - \tan^{-1}\left(\frac{f}{f_2}\right) - \tan^{-1}\left(\frac{f}{f_3}\right)$$

As $f \to \infty$, $\phi(t) = -90° - 90° - 90°$

$= -270°$.

Then the phase shifts of each stage of θ_1, θ_2 and θ_3 added together and give the total phase shift of an individual cases is

$\theta_1 = -\tan^{-1}\left(\frac{f}{f_1}\right)$

$\theta_2 = -\tan^{-1}\left(\frac{f}{f_2}\right)$.

$\theta_3 = -\tan^{-1}\left(\frac{f}{f_3}\right)$

If $f \to f_1 \Rightarrow \theta_1 = -\tan^{-1}\left(\frac{f_1}{f_1}\right)$

$= -45°$, θ_2 and θ_3 are negligible.

As $f \to f_2 \Rightarrow \theta_2 = -\tan^{-1}\left(\frac{f_2}{f_2}\right)$

$= -45°$, θ_1 and θ_3 are negligible but $\theta_2 = -45°$ and $\theta_1 = -90°$ so only θ_3 is negligible.

lly $f \to f_3 \Rightarrow \theta_3 = -\tan^{-1}\left(\frac{f_3}{f_3}\right)$

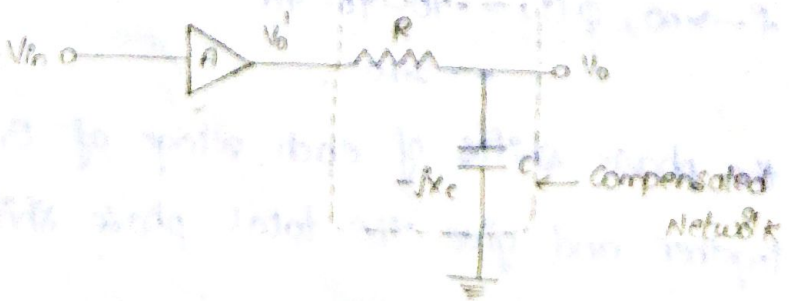
$= -45°$ $\theta_1 = -90°$ & $\theta_2 = -90°$.

Then the individual stage the total phase shift becomes -225°. This is an additional phase shift to 180° present b/w inverting terminal and o/p terminal. Due to that such additional phase shift the op-Amp may behaves oscillatory circuit and almost unstable.

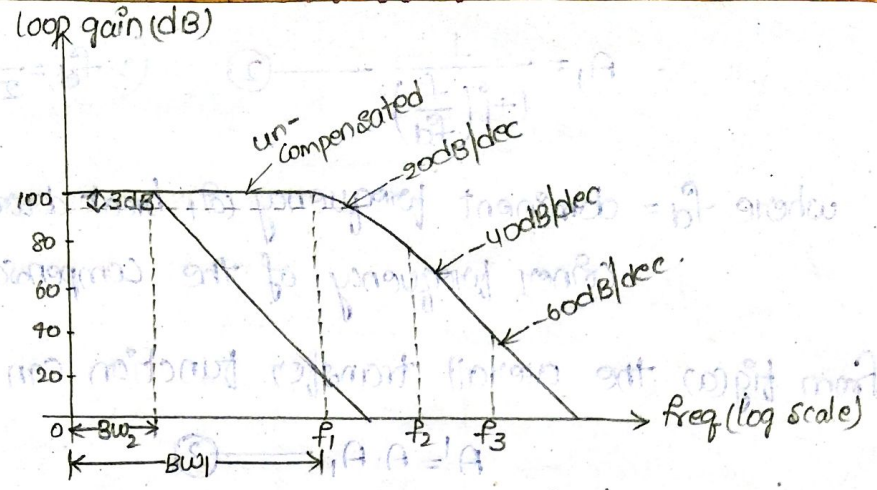
From the above observations individual stages of θ_1, θ_2 and θ_3. The min. +ve phase margin is produced at 180°-135°=45° and similarly at $f = f_3$ the -ve phase margin is observed at 180-225=-45°.

External Compensation:-

(i) Dominent-pole Compensation:-



(a) Dominent-pole compensation



Dominent-pole compensation means that the poles with magnitude much smaller than existing poles and hence the brake frequencies of the compensating network is the smallest compared with existing brake frequencies. Now consider an Op-Amp with brake frequencies and it's loop gain is

$$A = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]} \quad \text{---------} (1)$$

From fig(a) the dominent-pole is introduced by adding compensating network such as RC network. From that the transfer function can be expressed as

$$A_1 = \frac{V_o}{V_o'}$$

From the compensating network the voltage divider rule applied to the network it can be expressed as

$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_c}{R-jX_c}$$

W.K.T $\frac{1}{j} = -j$ and $X_c = \frac{1}{2\pi fc}$

$$A_1 = \frac{\frac{1}{j2\pi fc}}{R+\frac{1}{j2\pi fc}} = \frac{1}{1+j2\pi fRc}$$

$$\therefore A_1 = \frac{1}{1+j\left(\frac{f}{f_d}\right)} \quad \text{---(2)} \qquad \left(\because f_d = \frac{1}{2\pi RC}\right)$$

where f_d = dominent frequency (or) break down frequency (or) corner frequency of the compensating network.

From fig(a) the overall transfer function can be expressed as

$$A' = A \cdot A_1 \quad \text{---(3)}$$

Sub. eq (1) & (2) in eq (3)

$$= \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]} \times \frac{1}{1+j\left(\frac{f}{f_d}\right)}$$

$$\boxed{A' = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]\left[1+j\left(\frac{f}{f_d}\right)\right]}}$$

The values of R and C are selected in such a way that the loop gain becomes 0 decibels with a slope of -20dB/dec. This ensures that the phase shift is greater than 180° and produces a +ve phase margin. So we can observe that the 3dB down B.W is the non-compensated network system is B.W 1, while for compensated network it becomes B.W 2. That means the B.W drastically oreduces.

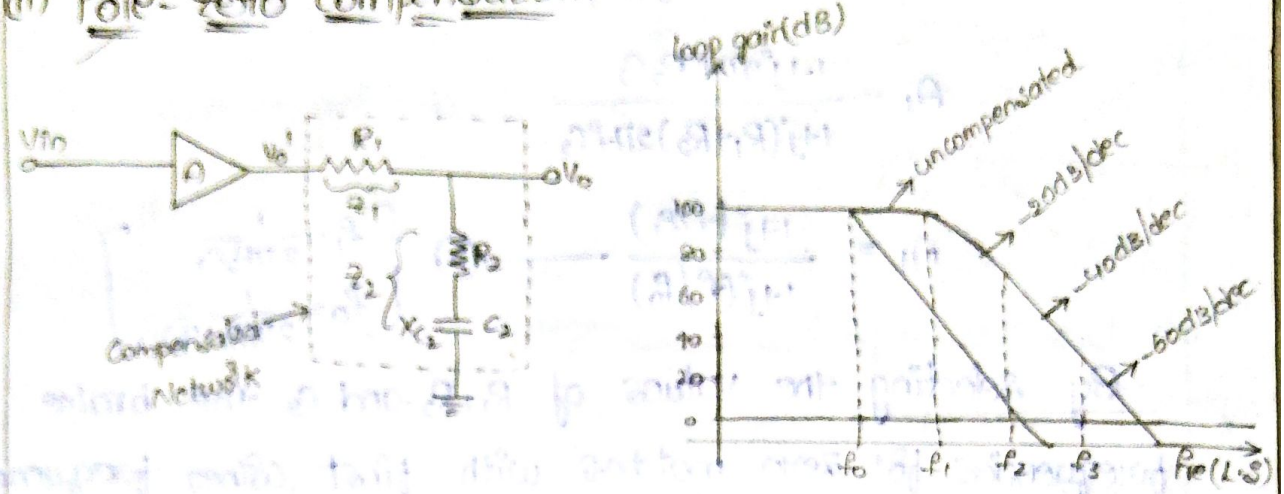
Advantages:-

1. Whenever a noise frequency components are produced with a small B.W, the noise immunity of the system can be improves.
2. Adjusting the value of f_d the phase margin and stability of the system is produced accurately.

Disadv:-

1 Only the disadvantage is the B.W drastically decreases.

(ii) Pole- zero Compensation:-



Consider the same Op-Amp described by the open loop gain (A) with 3 brake frequencies is

$$A = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]} \quad \text{---------- (1)}$$

By using this method the transfer function 'A' is modified by adding a pole and zero with the help of a compensating network. The zero is added at higher frequencies and a pole is added at lower frequencies. Then from fig (a) the transfer function of compensated network is

$$A_1 = \frac{V_o}{V_o'}$$

By using voltage divider rule it can be expressed as

$$A_1 = \frac{V_o}{V_o'} = \frac{Z_2}{Z_1+Z_2}$$

$$= \frac{R_2 - jX_{C_2}}{R_1+R_2-jX_{C_2}} \qquad \left[\because Z_1 = R_1,\ Z_2 = R_2 - jX_{C_2}\right]$$

W.K.T $\frac{1}{j} = -j$ and $X_{C_2} = \frac{1}{2\pi f C_2}$.

$$A_1 = \frac{R_2 + \frac{1}{j2\pi f C_2}}{R_1 + R_2 + \frac{1}{j2\pi f C_2}}$$

$$A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j(R_1 + R_2)2\pi f C_2}$$

$$A_1 = \frac{1 + j(f/f_1)}{1 + j(f/f_0)} \quad \text{——— (2)} \qquad \left[\because f_1 = \frac{1}{2\pi R_2 C_2},\ f_0 = \frac{1}{2\pi(R_1+R_2)C_2}\right]$$

By selecting the values of R_1, R_2 and C_2 the brake frequencies for zero matches with first corner frequency f_1 while the pole of the compensating network at f_0 is selected in such a way that the compensated transfer function A' passes through 0 decibels at 2nd corner frequency f_2 then the overall transfer function can be expressed as

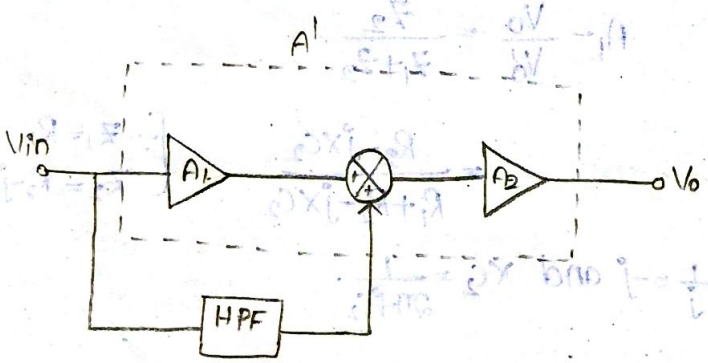
$$A' = A \cdot A_1 \quad \text{——— (3)}$$

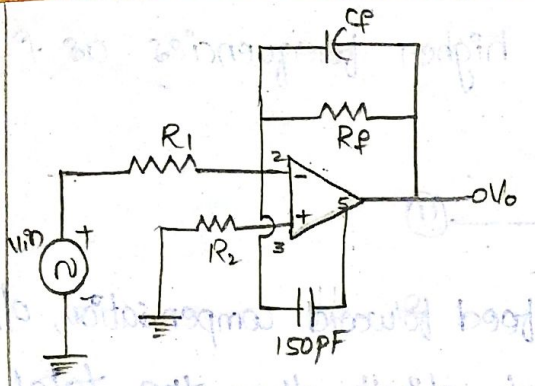
Sub (1) & (2) in eq (3)

$$= \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_1}\right)\right]\left[1+j\left(\frac{f}{f_2}\right)\right]\left[1+j\left(\frac{f}{f_3}\right)\right]} \times \frac{\left[1+j\left(\frac{f}{f_1}\right)\right]}{\left[1+j\left(\frac{f}{f_0}\right)\right]} \quad \text{where } 0 < f_0 < f_1 < f_2 < f_3$$

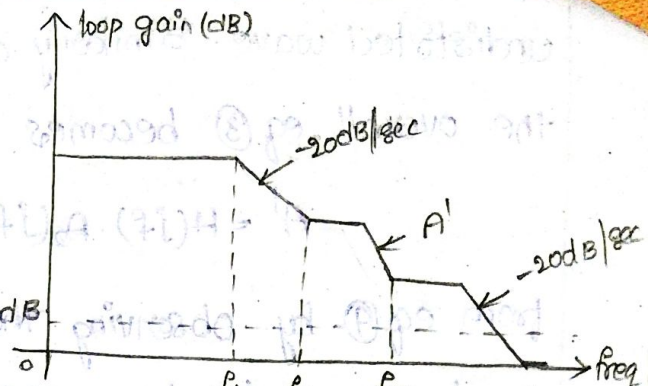
$$\therefore \boxed{A' = \frac{A_{OL}}{\left[1+j\left(\frac{f}{f_0}\right)\right]\left[1+j\left[\frac{f}{f_2}\right]\right]\left[1+j\left(\frac{f}{f_3}\right)\right]}}$$

20/8/18 **Feed forward Compensation:-**





(b) feedforw compensation



(c) effect of feed forward comp.

Feed forward compensation technique is used to reduce the drawback of dominent-pole compensation technique which is nothing but the drastical decreasing of B.W is overcome by using this technique.

This technique was implemented by combining two op-Amp's such as consider the high pass filter then the transfer function of high pass filter is

$$H(f) = \frac{j\left(\frac{f}{f_0}\right)}{1+j\left(\frac{f}{f_0}\right)} \quad \text{——— (1)}$$

From fig(a) the overall transfer function of feed forward compensation becomes

$$A' = (A_1 + H)A_2 \quad \text{——— (2)}$$

eq (2) was represented as in frequency response i.e;

$$A' = A_1A_2 + A_2H$$

$$= A + A_2H$$

$$A'(jf) = A(jf) + A_2(jf)\cdot H(jf) \quad \text{——— (3)}$$

from eq (3) at lower frequencies as $f \to 0$, the overall transfer function becomes

$$A' = 0$$

i.e; at lower frequencies this technique produces

undistorted wave. Similarly at higher frequencies as $f \to \infty$ the overall eq ③ becomes.

$$A' = H(jf) \cdot A_2(jf) \text{ ——— ④}$$

from eq ④ by observing the feed forward compensation, o/p graph was not decreases drastically then the total corner frequency for feed forward compensation.

$$f_0 = \frac{1}{2\pi R_i C_i}$$