UNIT-4

24/8/16

Transistor Characteristics

BJT (Bipolar Junction Transistor).

Introduction

→ In 1904-1947 mostly used in Electronic device is vaccum tube diode. In 1906 triode was used by adding a third element to the vaccum tube diode.

→ In 1920 pentode was introduced ie, 5 element device on December 23rd, 1947. 1st transistor was introduced at Bell laboratories by William Shockely.

→ Transistor is used for application purpose it can be used for either voltage or current Amplifier.

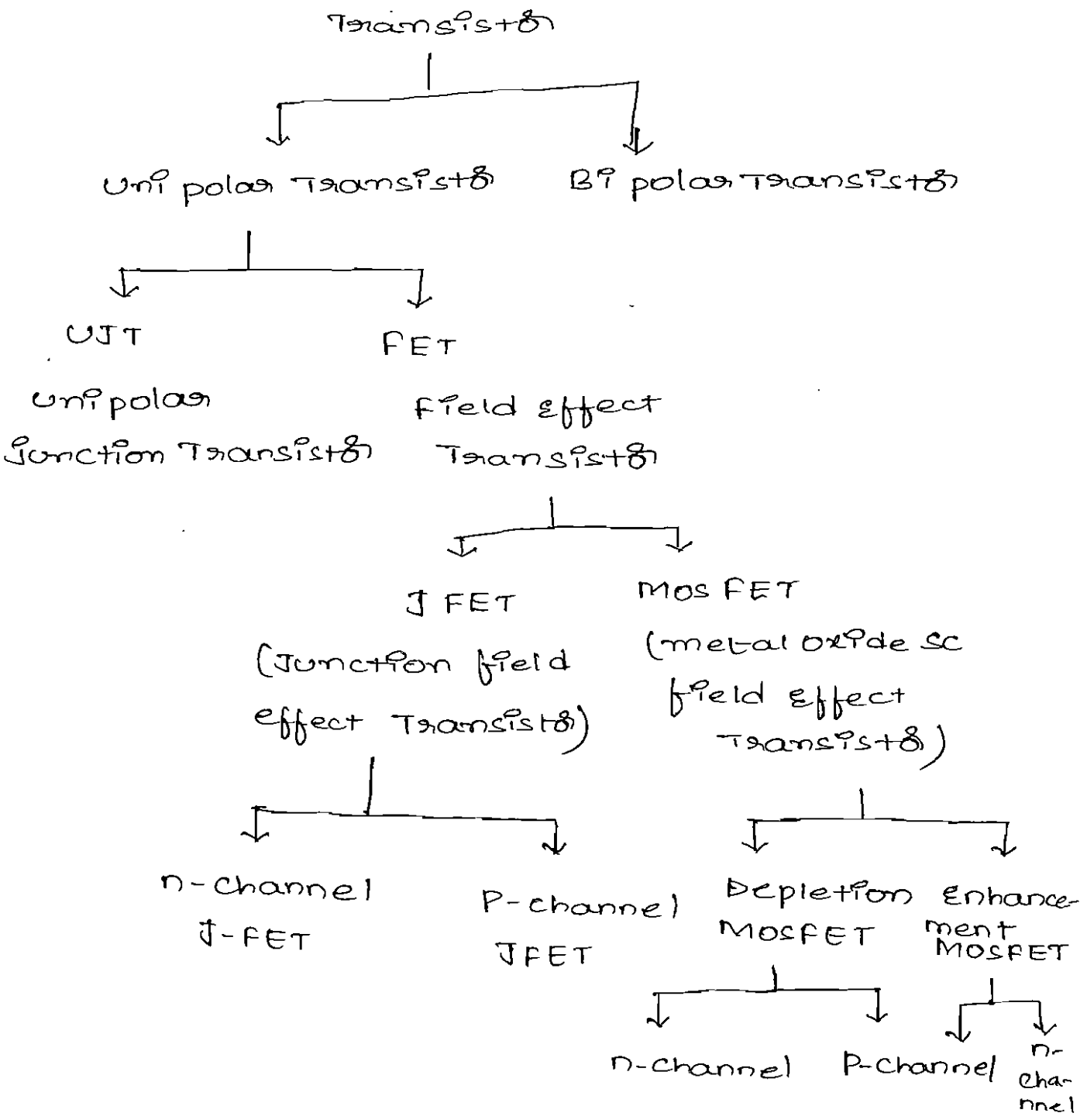
→ Transistor means transfer resistance ie signal are transferred from low resistance circuit (input) into high resistance circuit (O/p).

→ Transistors are used in amplifier, oscillators, and digital circuits.

Advantages

1. Smaller and light weight.
2. Rugged construction.
3. more Efficient
4. Less power consumption
5. Low operating voltages are possible

Classification of Transistors



→ Depending upon type of conduction transistors are classified into 2 types.

i) Uni polar Transistors (UJFET)

ii) Bi polar Transistors (BJT).

→ In uni polar transistors the conduction is due to majority charge carries only.

→ In Bi-polar transistor the conduction is due to both majority and minority charge carries.

BJT (Bipolar Junction Transistor)

→ BJT is a 3 terminal semiconductor device in which the operation depends on the interaction of both majority and minority carries and hence the name Bi polar the 3 terminals are

i) Emitter.

ii) Base

iii) collector.

i) Emitter:

→ The Left hand side section of the transistor is called Emitter.

→ The main function is to supply majority charge carries (either es or holes) to the base and it is more heavily dopped with a small cross sectional area.

ii) Base:

The middle section of transistor is called Base.

→ It is in blw the Emitter and collector.

→ It acts as a path for the moment of chare carriers. This region is lightly doped and thin layer and narrow cross section area.

iii) collector:

→ the right hand section of transistor is called collector

→ The main function of collector to collect majority charge carries through base.

→ This is moderately doped and having large cross sectional area.

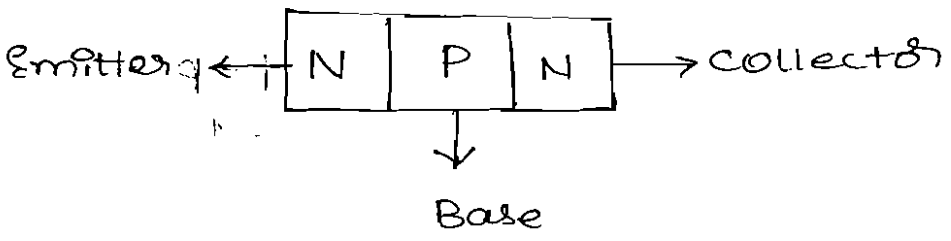
→ In most of the transistors collector region is made physically larger than the Emitter region due to large difference collector and Emitter are not interchangeble.

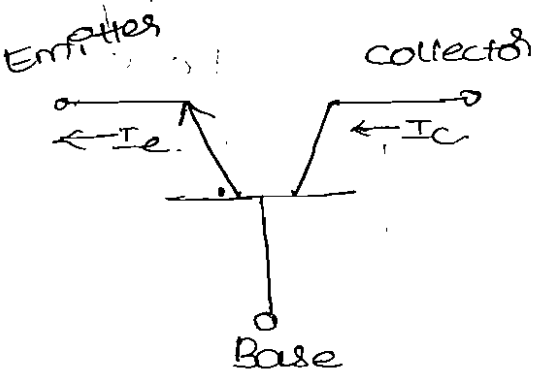
→ There are 2 types of BJT's

1. PNP
2. NPN.

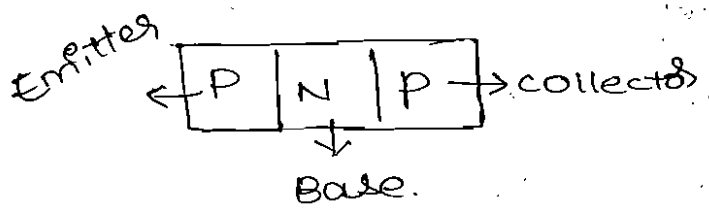
NPN Transistor

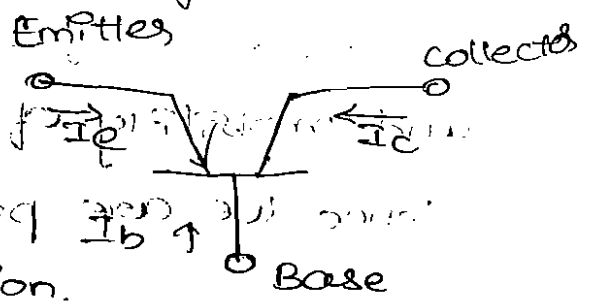
→ In NPN Transistor the p-type material is sandwiched blw 2 n-type material.





PNP Transistor: In P-n-P transistor, the n-type material is sandwiched blw two P-type materials.

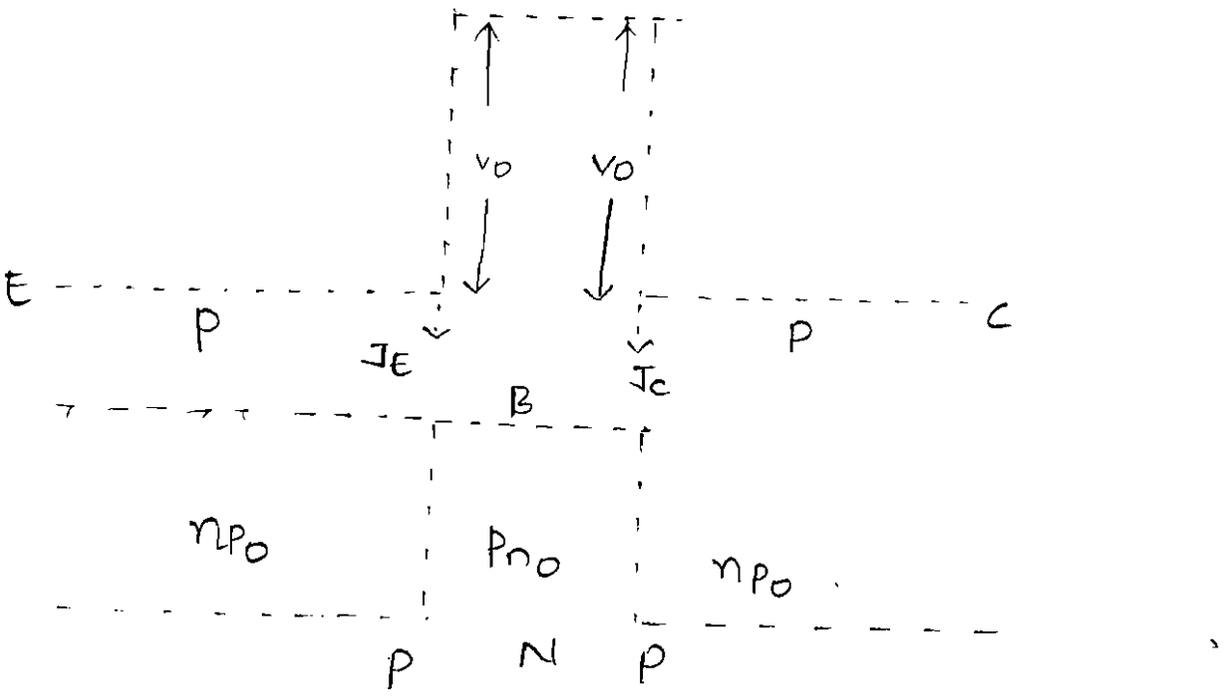




→ A transistor has two junction.

1. Emitter base Junction / Emitter Junction (JE).
2. collector – base Junction / collector Junction (Jc).

7/9/16 Open circuit & Unbiased Transistor (SA)



→ The charge carriers will be constant the charge carriers are at thermal equilibrium (initial stage). because there is no applied voltage so current is not flowing through it then the charge carriers will be constant.

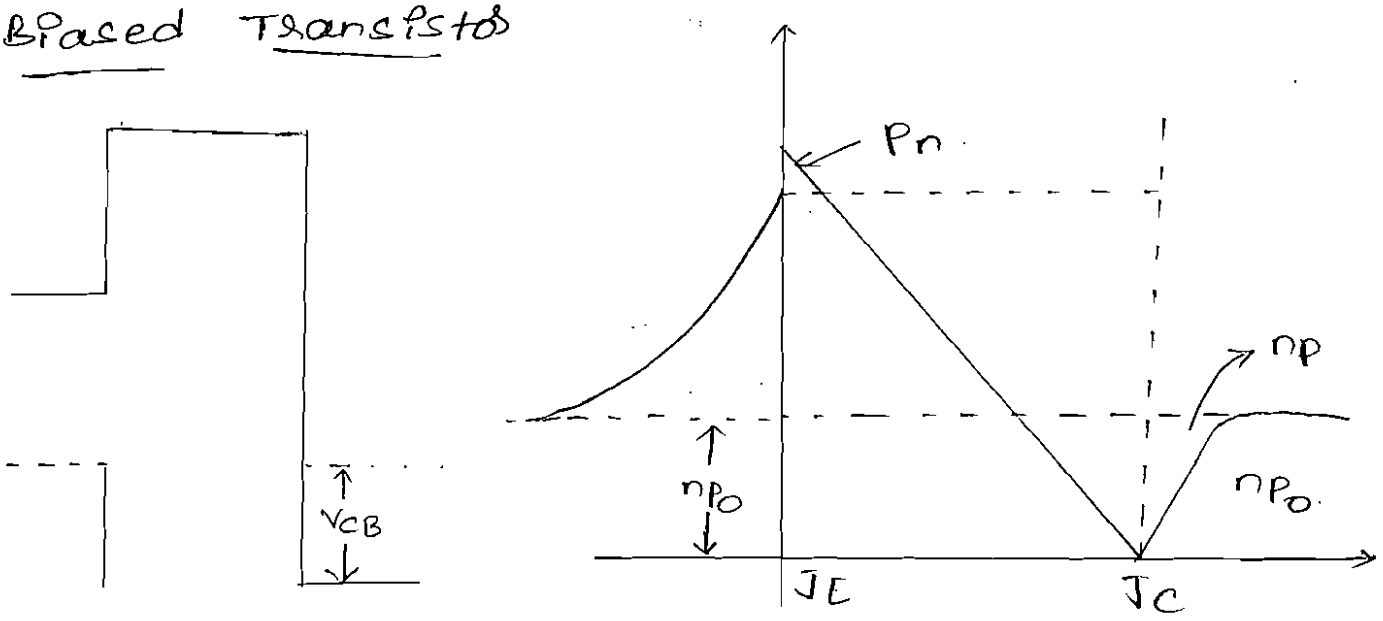
→ The npn Transistor became more popular than a pnp transistor because of the following reasons.

(i) A NPN Transistor is having n-type materials Electrons move faster than the holes.

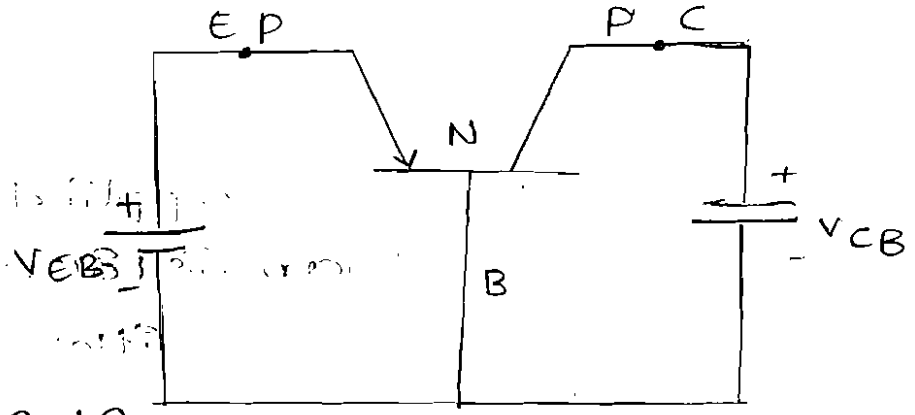
(ii) Carrier diffusion coefficient of Electrons (D_n) and mobility of electrons (μ_n) are high. and Hence we are preferable npn Transistor.

Reasons of Transistor

Biased Transistor



→ The transistor can be operated the following reasons based on type of biasing the Emitter and collector junction.



*Active & Linear:

→ The Emitter base junction is forward bias and collector base junction is reverse biased

~~**~~ Cutt off Regions:

→ The Emitter base junction and collector base junction are in Revease biased

* Saturations:

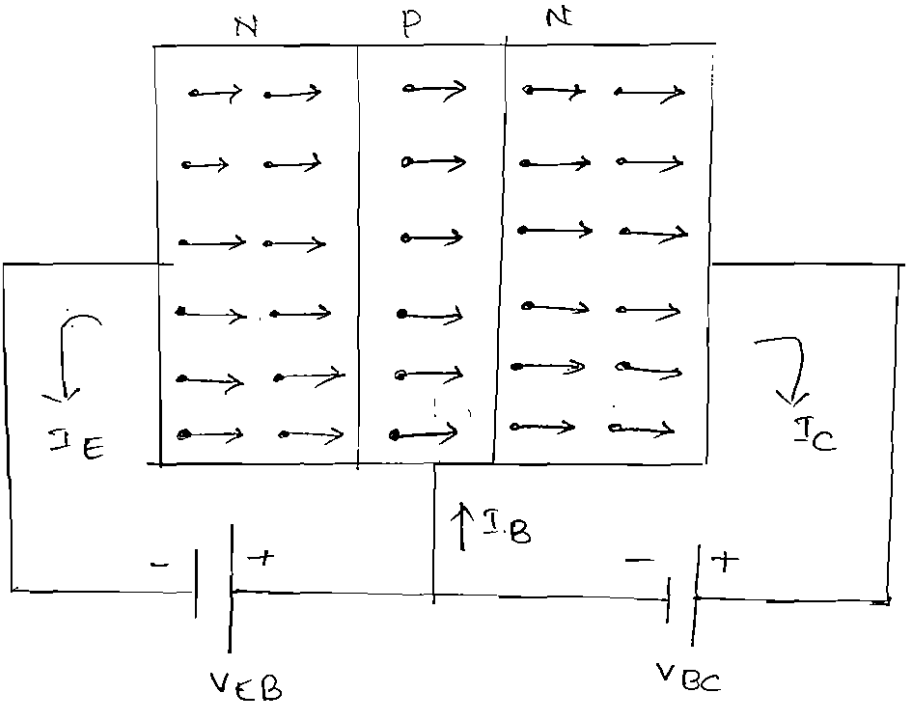
The Emitter base junction and collector base jun-

tion both are in forward bias.

* Inverted Region:

The Emitter base junction are in Reverse bias and Collector base junction are in forward bias.

Transistor current components (V.V.Imp).



Fig(a):

→ In fig(a) the forward bias is applied to Emitter base junction of npn transistor causes a lot of electrons from the emitter region to cross over the base region.

→ The base is lightly doped with p-type impurity the no. of holes in the base region is very small and hence the no. of electrons that combained with holes in the base region is also very small Hence a few electrons combained with holes to built & constitute a base current I_B.

→ The remaining e^- cross over into the collector region to constitute a collector current I_C.

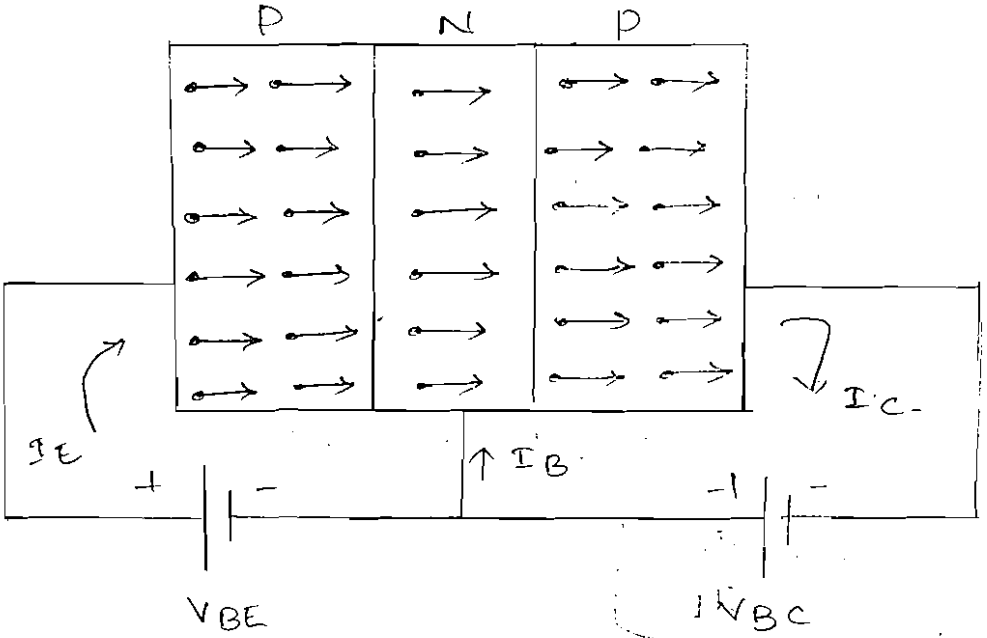
∴ The Emitter current $I_E = -(I_B + I_C)$

The magnitude of Emitter current $I_E = I_B + I_C$

This Eqn gives the fundamental relationship b/w the currents in a bipolar transistor circuit.

→ Always these fundamental Eqns shows the there are current amplification factors α, β in common base transistor configaration and common Emitter transistor configaration, common collector configarations.

Operation & current components of PNP Transistor



fig(a): current components of PNP transistor

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Emitter Efficiency (γ)

The EE is defined as concurrent of injected carriers at I_E to emitter junction to total Emitter current.

$$\gamma = \frac{I_E}{\text{Total Emitter current}}$$

$$\boxed{\gamma = \frac{I_E}{I_E}}$$

for pnp Transistor $\gamma = \frac{I_{pE}}{I_E}$

for npn " $\gamma = \frac{I_{nE}}{I_E}$

where I_{pE} = hole diffusion current at Emitter junction

I_{nE} = Electron diffusion current at Emitter junction

I_E = Total Emitter current

Total Emitter current $I_E = I_{PE} + I_{NE}$

$$\gamma = \frac{I_{PE}}{I_{PE} + I_{NE}}$$

for npn $\gamma = \frac{I_{NE}}{I_{PE} + I_{NE}}$

Transport factor (β)

It is defined as injected carrier current reaching collector junction (I_C) to injected carrier current at emitter junction (I_E).

$$\beta^* = \frac{I_{PC}}{I_{PE}}$$

Large signal current gain (α)

It is defined as the ratio of the -ve of the collector current implement to the emitter current change from zero to I_E as the large signal current gain of CB transistor.

$$\alpha = -\left(\frac{I_C - I_{CO}}{I_E}\right)$$

I_{CO} = Collector Current

I_C and I_E have opposite signal then α is always +ve. The typical value of α is 0.9 - 0.995. ie $\alpha \approx 1$

$$\alpha = \frac{I_{PC}}{I_E} \times \frac{I_{PE}}{I_{PE}}$$

$$I_{PC} = I_C - I_{CO}$$

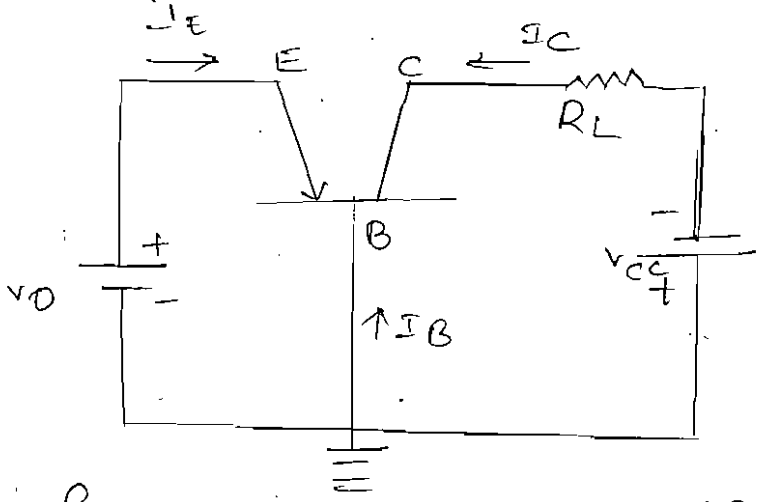
$$\alpha = \frac{I_{PC}}{I_{PE}} \times \frac{I_{PE}}{I_E}$$

$$\boxed{\alpha = \beta^* \times \gamma}$$

Applications Of Transistor

1. Transistor as an amplifier
2. Transistor as a Switch

1. Transistor as an amplifier



Fig(a): CB transistor configuration

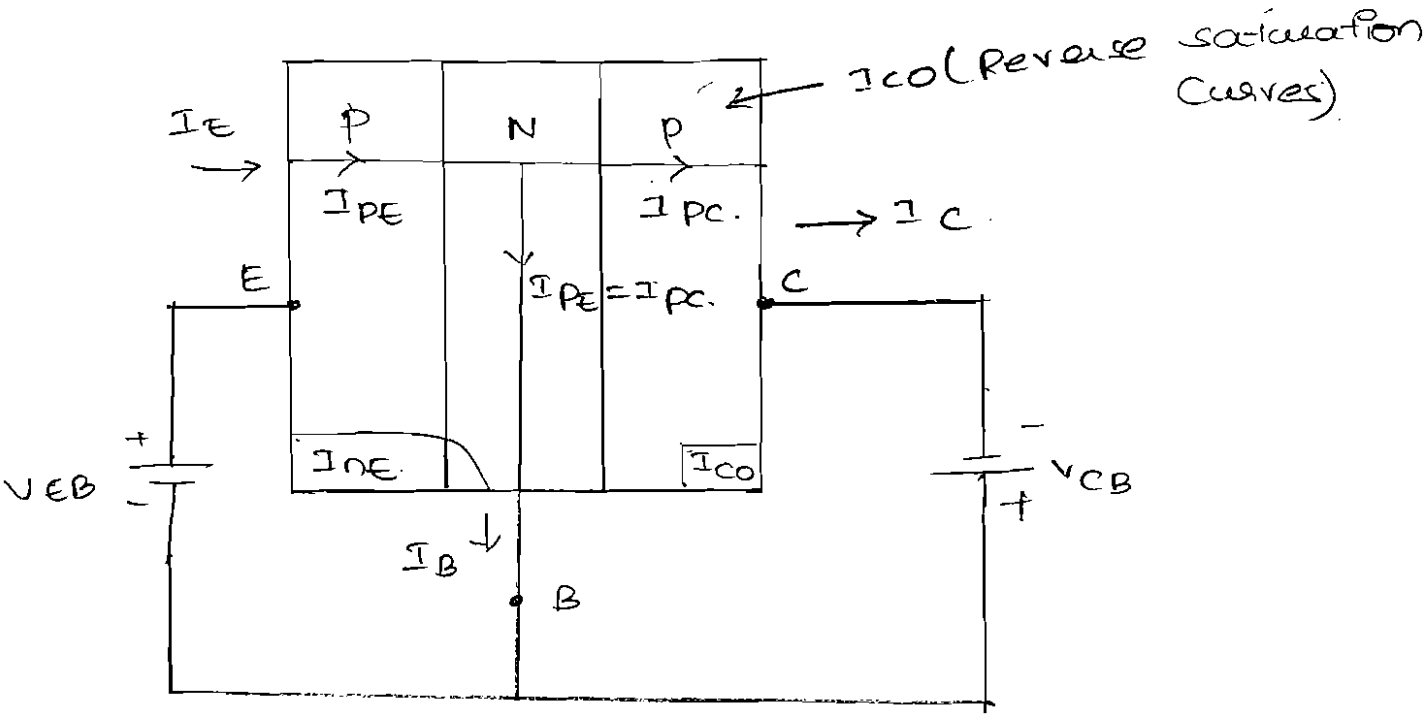
→ A load resistor R_L is connected in series with the collector supply voltage Vcc of CB transistor configuration as shown in fig a.

→ A small change in the input voltage b/w the emitter and base ie ΔV_i causes a large change in emitter current ie ΔI_E a fraction of these change in current is collected a passed through R_L and is denoted by symbol 'α'.

→ therefore the corresponding change in voltage across load Resistance R_L ie $\Delta V_0 = \Delta I_E \cdot R_L \cdot \alpha$

→ the voltage amplification $A_V = \frac{\Delta V_0}{\Delta V_i}$ is grately then unity and thus the transistor acts as amplify

Transistor current components.



I_{PE} = holes current due to the holes that are crossing from Emitter to base.

I_{nE} = Electron current due to the electrons that are crossing from base to Emitter

Total Emitter current $I_E = I_{PE} + I_{NE}$.

Base current $I_B = I_{PE} - I_{PC}$.

Collector current $I_C = I_{CO} - I_{PC}$.

Total Emitter current $I_E = I_B + I_C$.

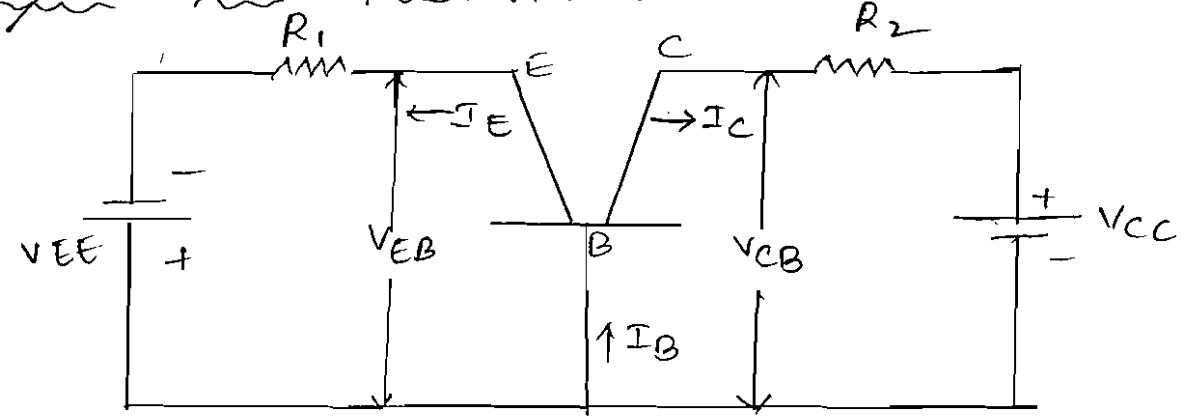
Transistor Configaration

The main application of transistor is an amplifier it circuit required two i/p terminals & o/p terminals but the transistor is a three terminal device so one terminal is common to both i/p & o/p depending on which terminal is making common the transistor can be operated the following three configaration.

1. Common base configaration
2. Common Emitter configaration

3- common collector configuration.

common base configuration



fig(a) :- CB configuration.

Mid Question

Early Effect & Base width modulations.

The type of configaration in which base terminal is common to both input and output terminals is called CB configaration & grounded base configaration.

Before going to discuss CB configaration It is better to know base width modulation.

Def: In the active region of transistor the Emitter Junction is forward biased and Collector junction is reverse bias with Reverse voltage V_{CB} increases the width of the depletion region. At collector junction increases which in term reduces the width of base region the variation of width of depletion region at Emitter Junction is negligibable compare with the collector junction finally increasing the V_{CB} Effect to Base width reduces it is called the base width modulation & Early effect.

$$V_B = \frac{2N_A}{2\varepsilon} W^2$$

Where

W = space charge region width

effects of base width modulation:

* Recombination of charge carriers with in the base region reduces so the base current decreases
* Concentration of minority carriers increases. So emitter current increases
* for large reverse voltage the width of the base becomes zero causing voltage breakdown in the transistor. This phenomenon is known as punch through (or) reach through

current amplification factor(α):-

It is defined as the ratio of change in collector current to base current at constant V_{CB} It is denoted by α_{AC}

$$= \frac{\Delta I_C}{\Delta I_E} \Big| V_{CB} = \text{constant}$$

$$\alpha_{DC} = \frac{I_C}{I_E} \Big| V_{CB} = \text{constant}$$

$$\alpha_{DC} = \frac{I_C}{I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C \rightarrow (1)$$

Divide eq (1) ΔI_E

$$\frac{\Delta I_E}{\Delta I_E} = \frac{\Delta I_B}{\Delta I_E} + \frac{\Delta I_C}{\Delta I_E}$$

$$1 = \frac{\Delta I_B}{\Delta I_E} + \alpha_{AC}$$

$$\alpha = 1 - \frac{\Delta I_B}{\Delta I_E}$$

$$\alpha = 0.9 \text{ to } 0.995$$

$$\boxed{\alpha \cong 1}$$

xpression for collector current :

I_{CBO} = very small leakage current

large % of emitter current that reaches the collector terminal

i.e αI_E

$$\alpha = \frac{I_{CO} - I_C}{I_E} \qquad (I_{CO} = I_{CBO})$$

$$I_C = \alpha I_E + I_{CBO}$$

where I_{CBO} = reverse saturation current (or) leakage current

$$I_E = \alpha (I_B + I_C) + I_{CBO}$$

$$I_E = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO} \rightarrow (1)$$

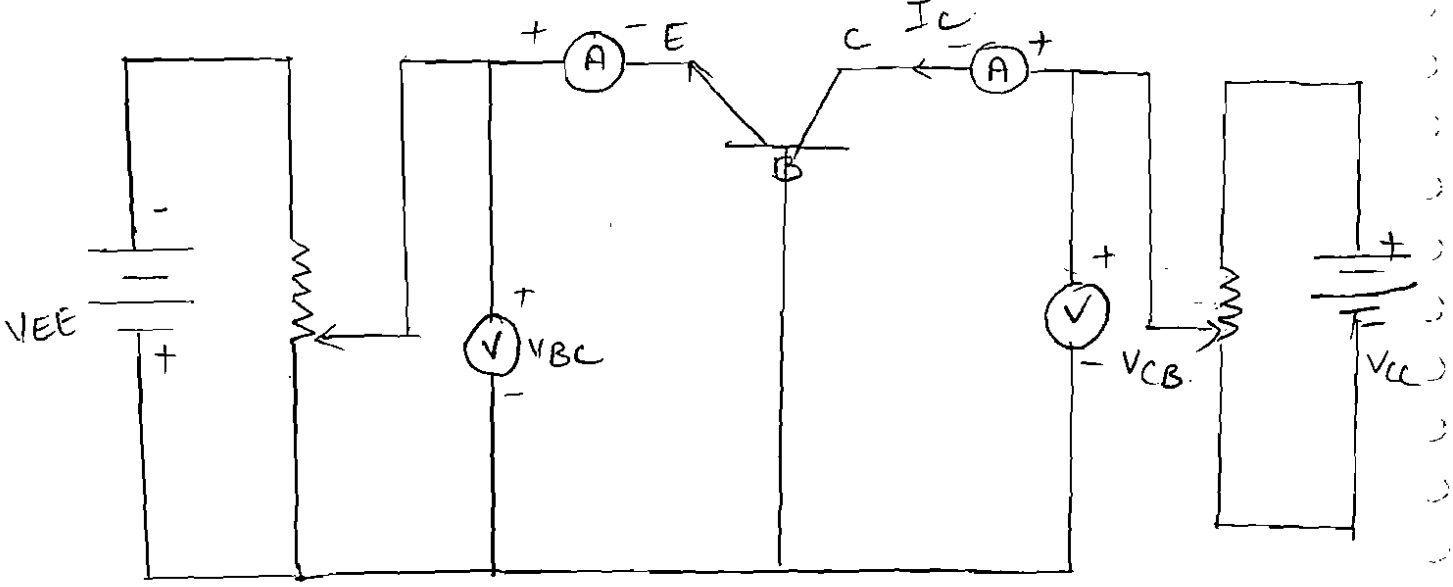
eq (1) divided by $(1-\alpha)$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$\boxed{I_C = \beta I_B + (1+\beta) I_{CBO}}$$

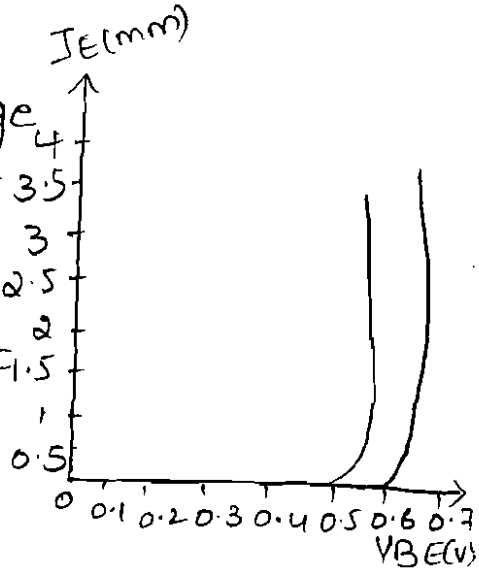
where $\boxed{\beta = \frac{\alpha}{1-\alpha}}$

CB characteristics :



i/p characteristics:

for input characteristics first fix the voltage V_{BC} say that 2v now vary the voltage V_{EE} slowly in steps of 0.5v and notedown the current I_E for each value of V_{BE} and plot the graph for I_E and V_{BE}



o/p characteristics:

for output characteristics first fix the current I_E say that 0 uA now vary the voltage V_{cc} slowly in steps of 0.5 volts and note down the current I_C for each value of V_{BC}

plot the graph $V_i = f_1(I_i, V_o)$

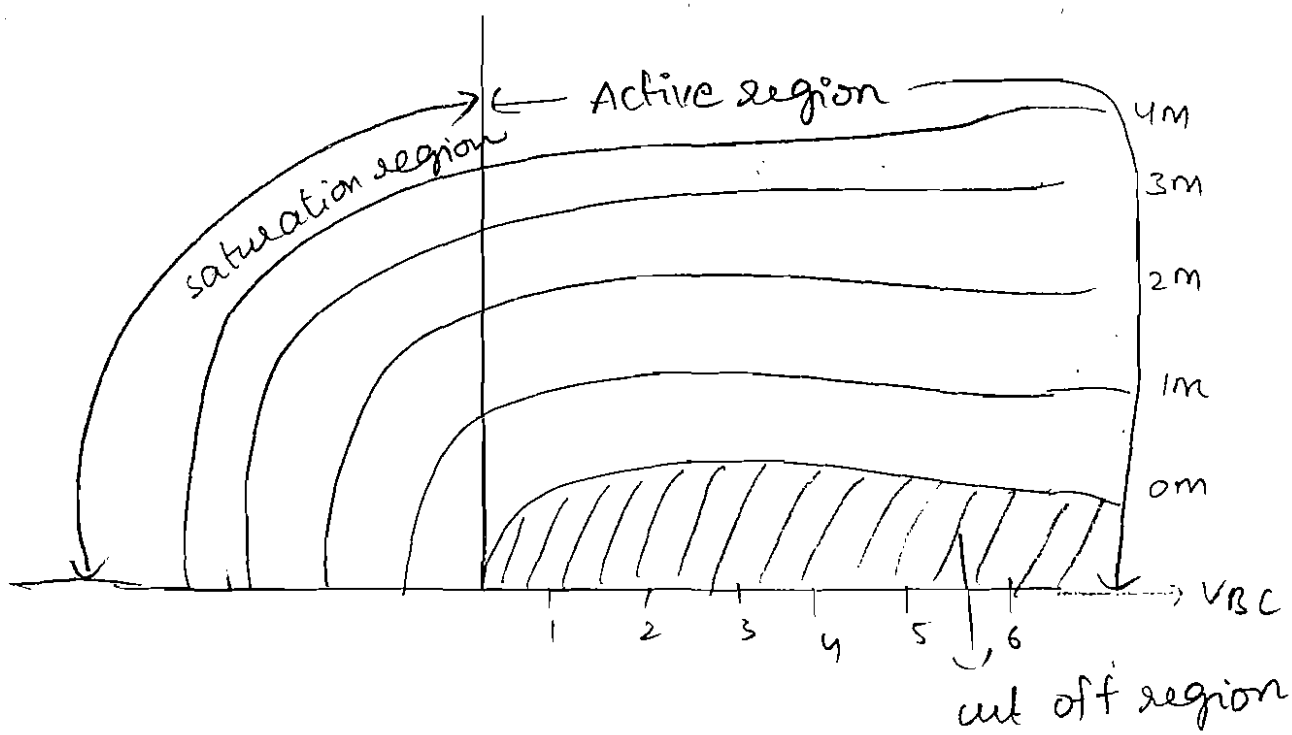
$$I_o = f_2(I_i, V_o)$$

from hybrid parameters $V_i = h_{11} I_i + h_{12} V_o$

$$I_o = h_{21} I_i + h_{22} V_o$$

$$h_{12} = V_i / V_o \,|\, I_i = \text{const}$$

$$h_{22} = I_o / V_o \,|\, I_i = \text{const}$$



NOTE: BJT is a current control device due to the analysis of H-parameters

Output characteristics have three regions

1. cut off region
2. active region
3. saturation region

below x axis is called cut off region

In Active region $I_C = \alpha I_E + I_{CBO}$

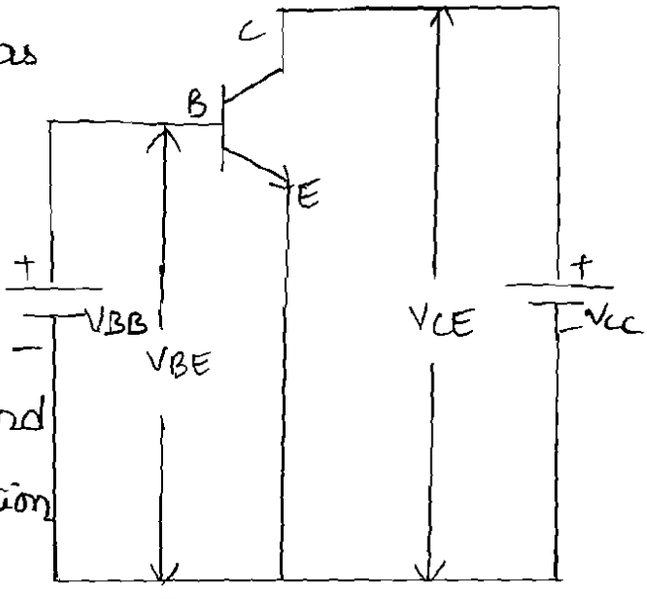
I_{CBO} = small reverse saturation (or) leakage current

It is very small current it is neglected so $I_C = \alpha I_E$

CB configuration doesnot work voltage amplifier and CB configuration doesnot proper practically.

CE configuration:

The CE circuit for NPN transistor as shown in fig(a). The i/p is taken as the base & emitter and the o/p is connected blw emitter and collector. Since the emitter transistor is common to both i/p and o/p. Hence the name CE configuration



fig(a) CE configuration

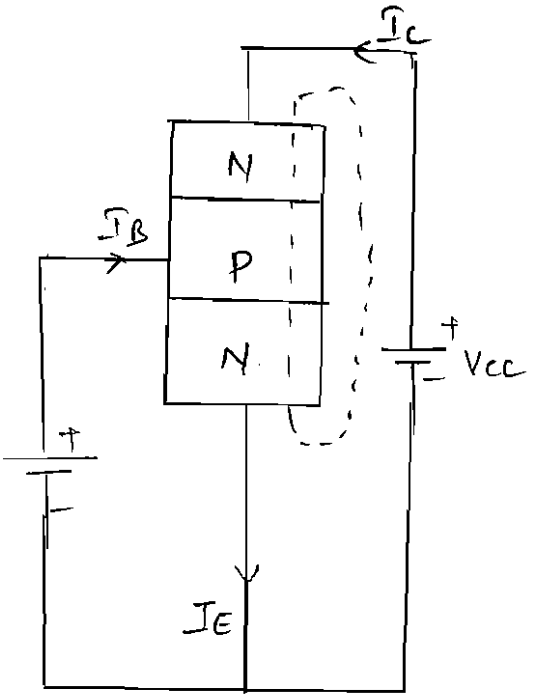
Current amplification factor:

The amplification factor defined as the ratio of collector current to base current

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

expression for collector current:



W.K.T $I_C = \alpha I_E + I_{CBO}$

$I_C = \alpha(I_B + I_C) + I_{CBO}$

$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \rightarrow (1)$

from the figure

$I_C = \beta I_B + I_{CEO} \rightarrow (2)$

Compare eq (1) & (2)

$I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$

$\beta = \frac{\alpha}{1-\alpha}$

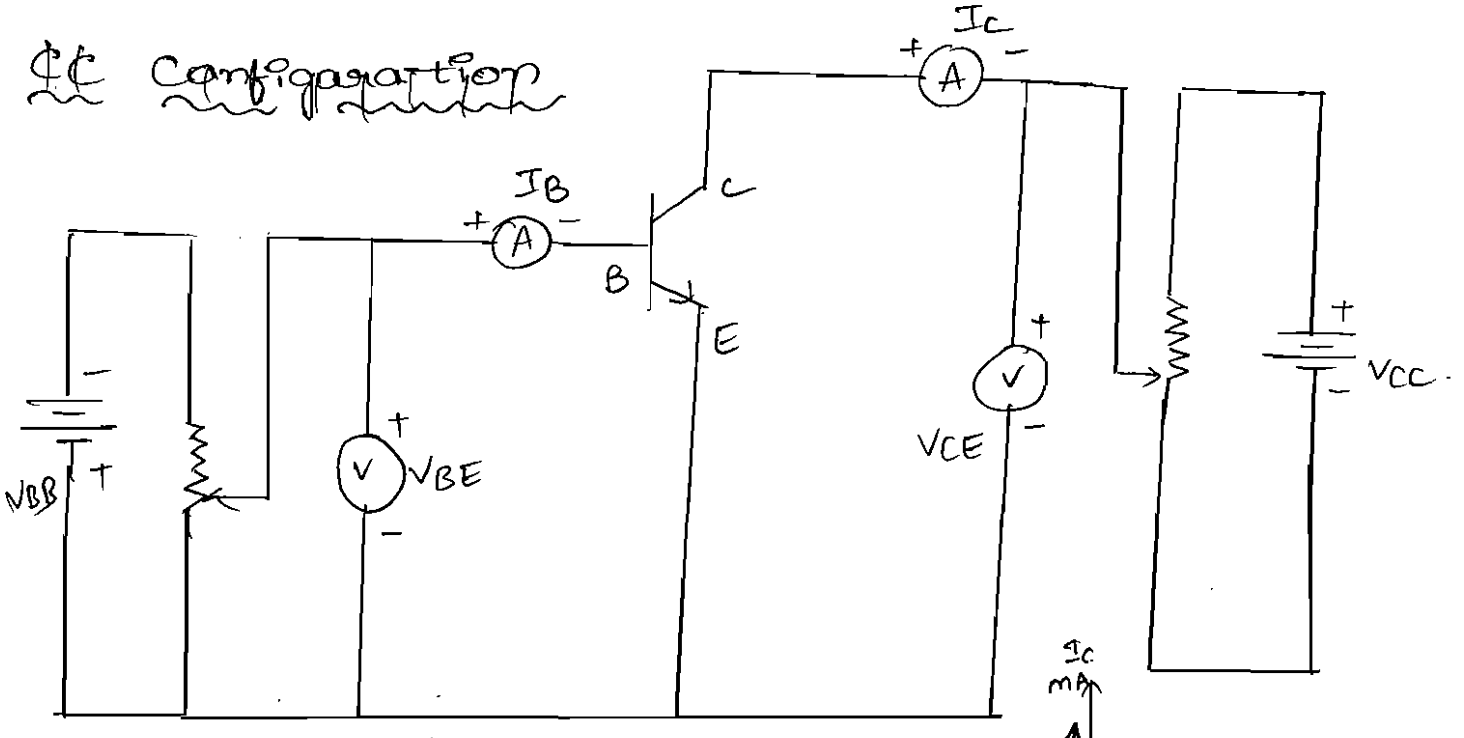
$I_C = \beta I_B + (1+\beta) I_{CBO}$

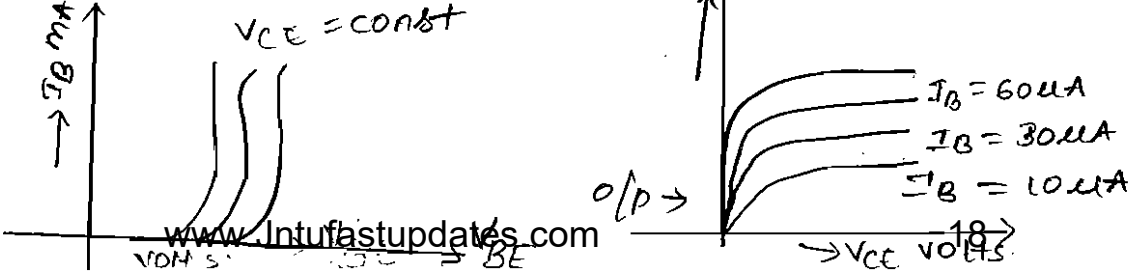
'β' ranges from 50 to 400

when I_{CEO} = leakage current (or) reverse saturation current when the i/p is open ($I_p = 0$)

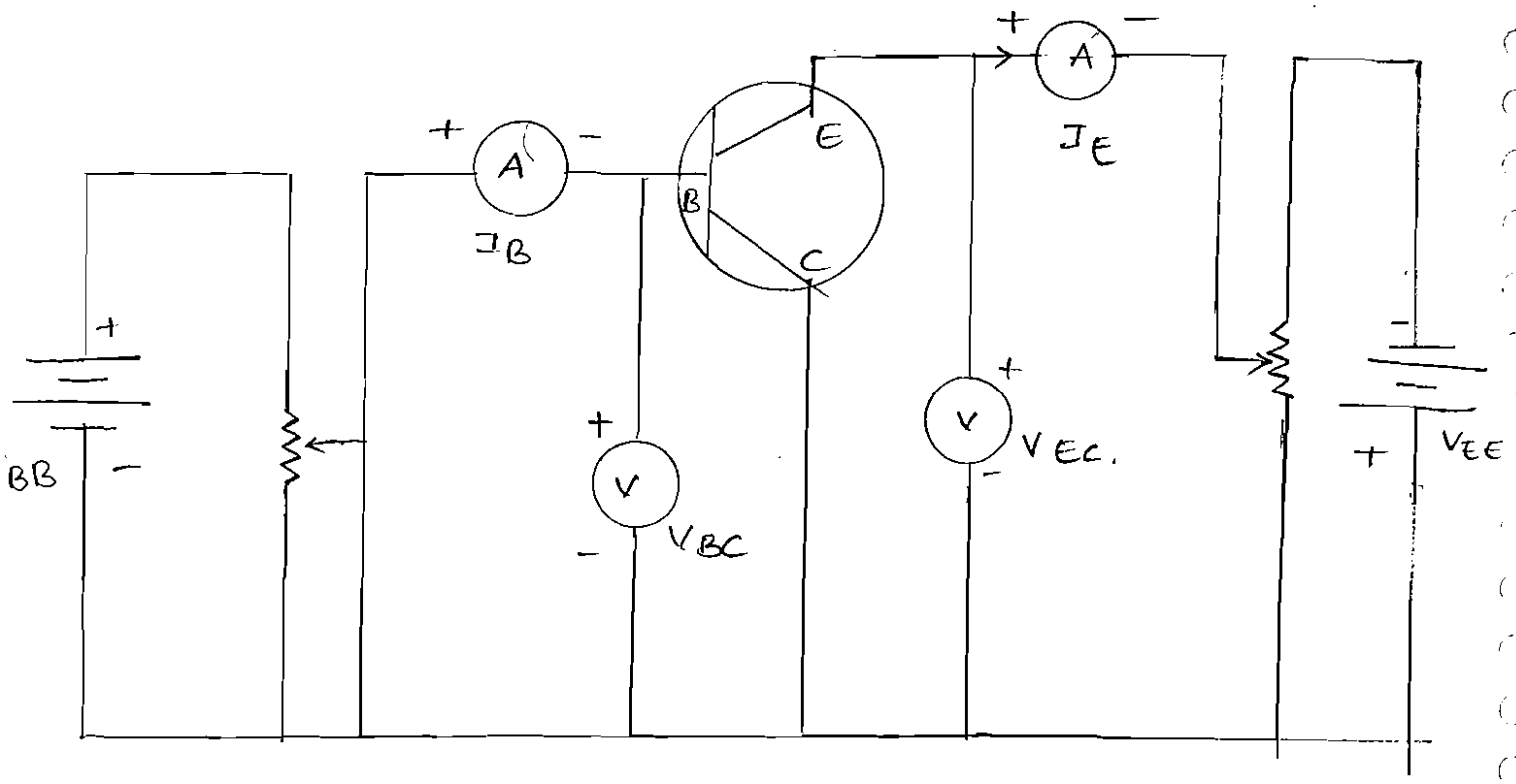
CE characteristics:

CE Configuration



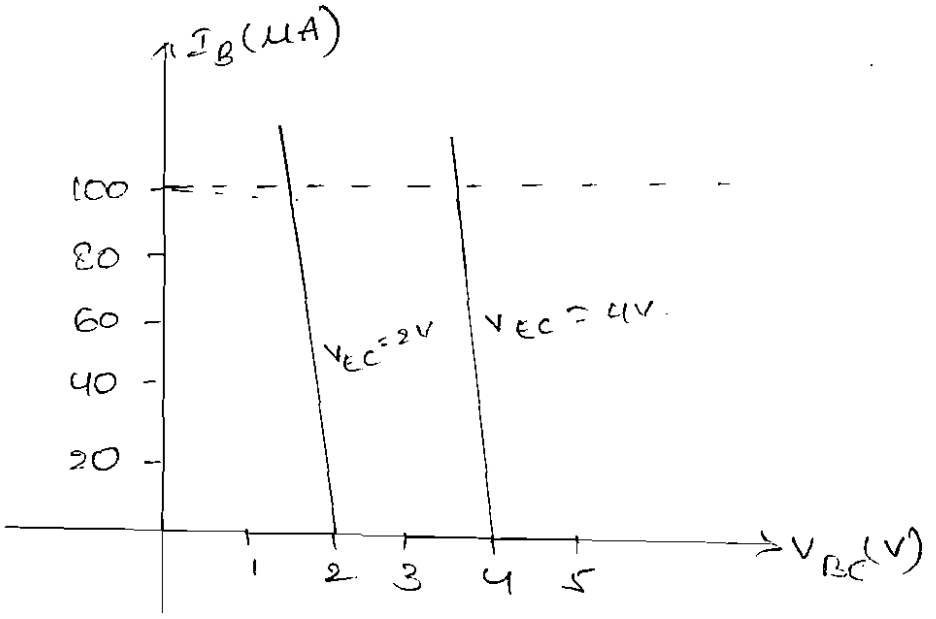


CC configuration



Fig(a): Circuit determine CC static characteristics

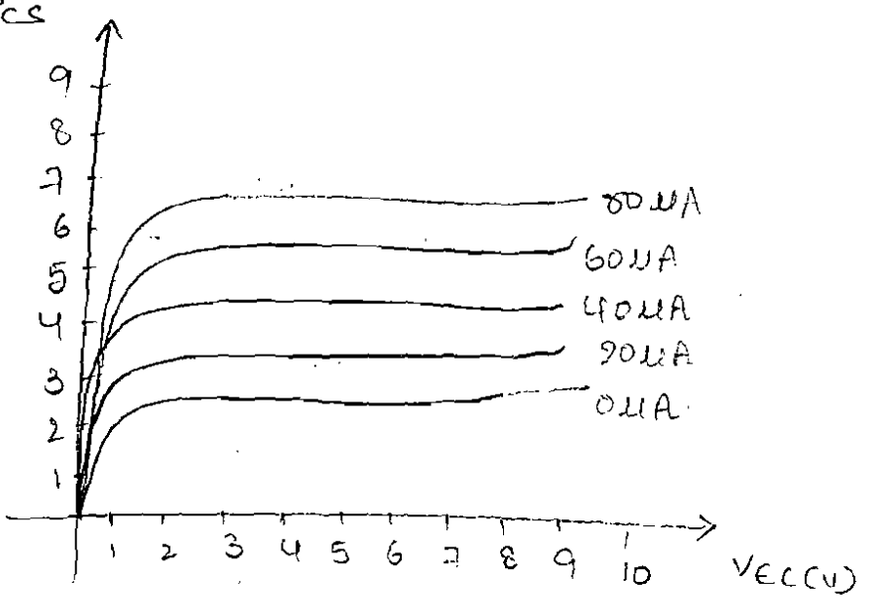
I/p characteristics



To determine the i/p characteristics V_{CC} is kept at a suitable fixed value. The base collector voltage V_{BC} is increased in equal steps and corresponding increases in I_B is noted. This is repeated

for different fixed values of V_{EC} plots of V_{BC} Vs I_{BE} for different values shown in fig (b) are the i/p characteristics

O/p characteristics



Current amplification factor(γ)

The current amplification factor is defined as the ratio of emitter current to base current

$$\gamma_{AC} = \frac{I_E}{I_B}.$$

$$\gamma_{DC} = \frac{\Delta I_E}{\Delta I_B}.$$

In CB configuration α is $\frac{\Delta I_C}{\Delta I_E}$

In CE configuration β is $\frac{\Delta I_C}{\Delta I_B}$

In CC configuration γ is $\frac{\Delta I_E}{\Delta I_B}$

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* Relation between α, β, γ. (Imp).

→ α = common base short circuit Amplification factor & Large signal current gain of the Transistor in CB configaration.

β = Common Emitter forward current amplification factor & Large signal current gain of transistor in CE configaration.

γ = Large signal current gain of transistor in CC configaration.

We know that $I_E = I_B + I_C$

$$I_B = I_E - I_C$$

$$\alpha = \frac{I_C}{I_E}$$

We know that $I_E = I_B + I_C$.

$$\alpha = \frac{I_C}{I_B + I_C} \longrightarrow (1)$$

⟹ Divide Eq (1) by I_B.

$$\alpha = \frac{\frac{I_C}{I_B}}{1 + \frac{I_C}{I_B}}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}} \quad \left(\because \beta = \frac{I_C}{I_B}\right)$$

$$\alpha = \frac{I_C}{I_E} \quad \left(\because I_E = I_B + I_C \right.$$
$$\left. I_C = I_E - I_B\right)$$

$$\alpha = \frac{I_E - I_B}{I_E} \longrightarrow (2)$$

Divide Eqn (2) by I_B.

$$\alpha = \frac{\frac{I_E}{I_B} - 1}{I_E / I_B}$$

$$\boxed{\alpha = \frac{\gamma - 1}{\gamma}} \quad (\because \gamma = I_E / I_B).$$

$$\longrightarrow \beta = \frac{I_C}{I_B} \qquad (I_E = I_B + I_C)$$

$$= \frac{I_C}{I_E - I_C} \qquad (\because I_B = I_E - I_C)$$

Divide by I_E

$$= \frac{I_C / I_E}{I_E / I_E - I_C / I_E}$$

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}} \quad (\because \alpha = I_C / I_E)$$

$$\beta = \frac{I_E}{I_B}$$

$$\beta = \frac{I_E - I_B}{I_B}$$

$$= \frac{I_E / I_B - 1}{I_B / I_B} \qquad (\text{Divide By } I_B)$$

$$\boxed{\beta = \gamma - 1} \quad (\because I_E / I_B = \gamma)$$

$$\longrightarrow \gamma = \frac{I_E}{I_B}$$

$$= \frac{I_E}{I_E - I_C}$$

$$= I_E / I_E \;/\; I_E / I_E - I_C / I_E \qquad (\text{Divide by } I_E)$$

$$\gamma = \frac{\alpha}{\alpha - 1}$$

$$\therefore \gamma = \frac{1}{1-\alpha} \quad (\because \alpha = I_C / I_E)$$

$$\gamma = \frac{I_E}{I_B}$$

$$= \frac{I_C + I_B}{I_B} \quad (\text{Divide by } I_B)$$

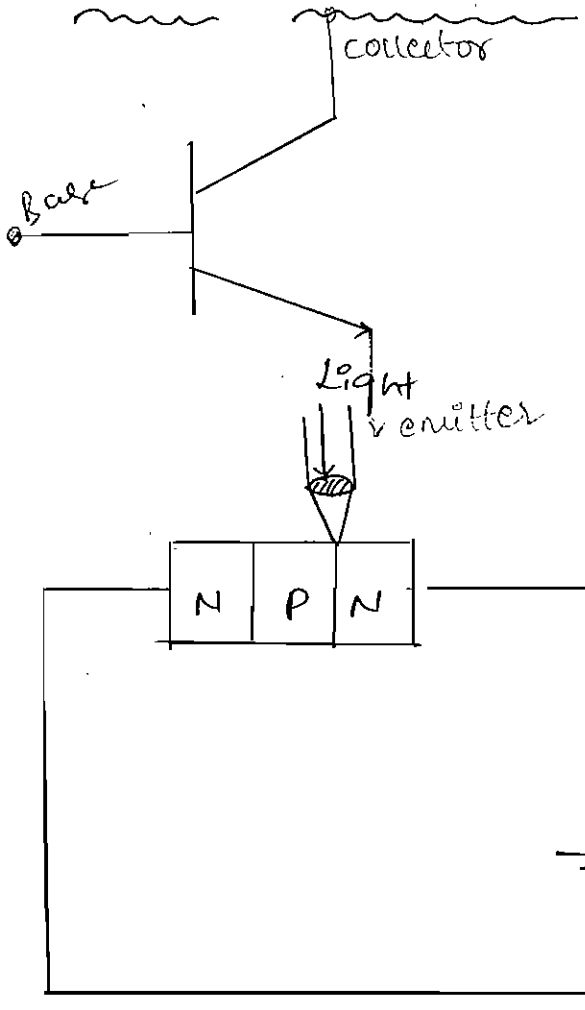
$$= \frac{I_C / I_B + 1}{I_B / I_B}$$

$$= \frac{\beta + 1}{1}$$

$$\gamma = 1 + \beta \quad (\because \beta = I_C / I_B).$$

* PHOTO TRNSISTOR

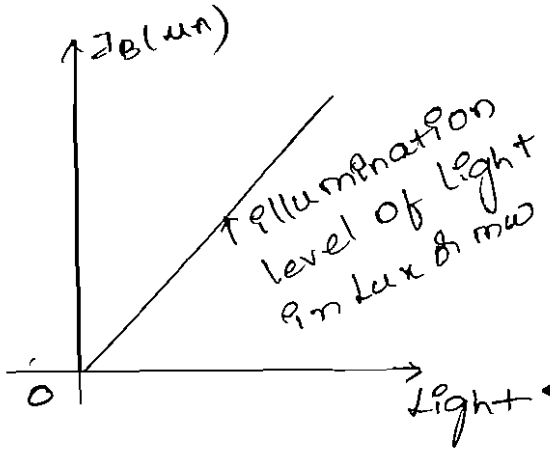
1 Lux = 0.92 milliwatts

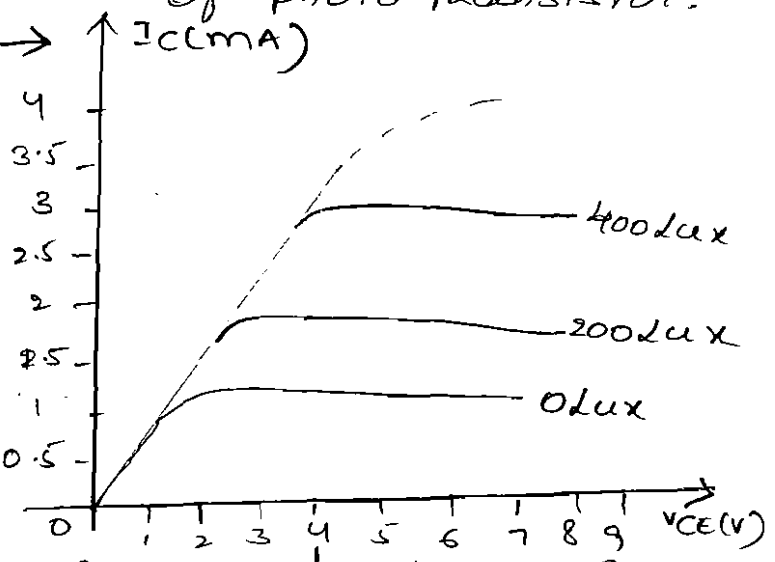


fig(a): NPN photo transistor symbol.

fig(b): photo transistor biasing arrangement

fig(c): I/p characteristics of photo Transistor.





fig(d): O/P characteristics

* Applications

1. Highspeed reading of punched cards & tapes
2. Light detection systems.
3. Light operated switches.
4. Reading of film sound track.

* Typical Transistor voltage values

Type	V_{BE}(sat)	V_{BE}(sat)	V_{BE}(Active)	V_{BE}(cutin)	V_{BE}(cutoff)
Silicon	0.8	0.7	0.6	0.5	0
Germanium	0.1	0.3	0.2	0.1	−0.1

In CE configuration $V_{BE} \geq 0.7$ volts (active region)
≤ 0.7 volts (cut off region)

Problems

1. In common base transistor circuit the Emitter current (I_E) is 10milliAmperes and I_C is 9.5mA. find the value of base current I_B.

Sol:- $I_B = I_E * I_E - I_C$

$= 10 - 9.8$

$= 0.2mA$.

2. The common base DC current gain of Transistor is 0.96. If the Emitter current is 10mA what is the value of Base current.

Sol:- $I_C = I_B + I_E$

Given $\alpha = \frac{I_C}{I_E}$

$\alpha = 0.96, I_E = 10mA$

$\alpha \Rightarrow 0.96 = \frac{I_C}{10mA}$

$I_C = 10 \times 0.96 mA$

$I_C = 10 \times 0.96 \times 10^{-3} A = 9.67mA$

$I_B = I_E - I_C$

$= 10mA - 9.67mA$

$= 0.33mA$.

3. The transistor has $I_E = 10mA$ and $\alpha = 0.98$. Determine the value of I_C and I_B.

4. If a transistor has α of 0.97. Find the value of β. If $\beta = 200$ find the value of α.

$$\beta = \frac{\alpha}{1+\alpha} = \frac{0.97}{1-0.97} = 32.33$$

$$\alpha = \frac{\beta}{1+\beta}$$

$$\alpha = \frac{200}{200+1}$$

$$\boxed{\alpha = 0.99}$$

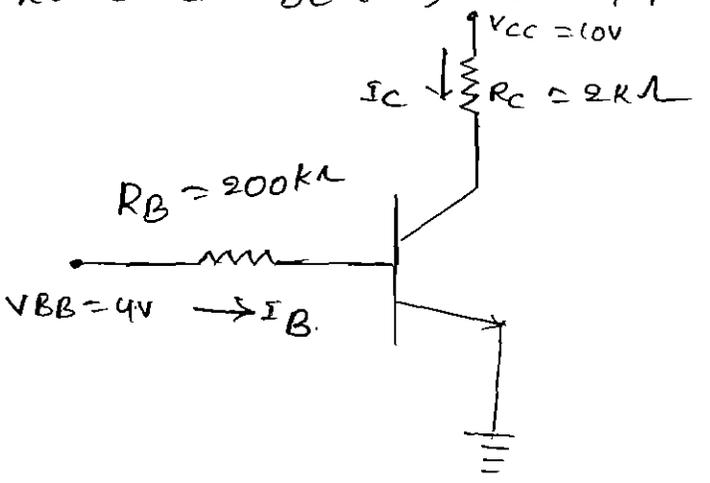
5. A transistor has $I_B = 100mA$ and $I_C = 2mA$ then find i) β of the transistor ii) α of the transistor iii) Emitter current I_E iv) If I_B changes by $+25mA$ and I_C changes by $+0.6mA$ find the new value of β.

6. For a transistor circuit having $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5$ micro A and $I_B = 100\mu A$. Find I_C & I_E

7. If $\alpha_{DC} = \frac{I_C}{I_E} = 0.99$ and $I_{CBO} = 50\mu A$. find I_E (Emitter current).

(8)*. Determine the base, collector and Emitter currents and V_{CE} for CE circuit shown in below fig for $V_{CC} = 10V$ and $V_{BB} = 4V$, R_B (Base Resistance) $= 200k\Omega$

$R_C = 2\,K\Omega$ and $V_{BE}(on) = 0.7V$, $\beta = 200$



Sol:-

The base current $I_B = \dfrac{V_{BB} - V_{BBE(on)}}{R_B}$

$= \dfrac{4 - 0.7}{200} = \dfrac{3.3}{200}$

$= 16.5\,m\mu A$.

The collector current $I_C = \beta I_B$

$= 200 \times 16.5$

$= 3,300.$

$= 3.3\,mA$

Emmitter Current $I_E = I_B + I_C$

$= 16.5\,\mu A + 3.3\,mA$

$= 3.3165\,mA.$

$V_{CE} = V_{CC} - I_C R_C$

$= 1 - 3.3 \times 2\,K\Omega$

$= 10 - 6.6$

$= 3.4V$

$V_{CE} = 3.4V$

(9). The Reverse voltage current of the transistor when connected in CB configuration is 0.2μA and it 18μA when the same transistor is connected in CE configuration. Calculate α_{dc} and β_{dc} of the transistor.

Sol:- $I_{CBO} = 0.2\mu A$, $I_{CEO} = 18\mu A$

$I_{CBO} = (1+\beta) I_{CBO}$

$$\beta = \frac{I_{CEO}}{I_{CBO}} - 1$$

$$= \frac{18\mu A}{0.2\mu A} - 1$$

$$\boxed{\beta = 89}$$

$$\alpha = \frac{\beta}{1+\beta}$$

$$= \frac{89}{90}$$

$$\boxed{\alpha = 0.988}$$

BJT Disadvantages

It also has low i/p impedence.

considerable noise present at the o/p.

Transistor these drawbacks has been overcome to introduced FET.

*FET [Field Effect Transistor]

→ FET is developed in the Early 1960 is an another semiconductor device like a BJT it can be used as amplifier or switch.

Advantages Of FET over BJT

→ FET is a unipolar device ie conduction of the device depends only on the single charge carriers, where as BJT is a bipolar device ie conduction of the device depends on both charge carriers.

→ FET has high i/p impedance in the orders of OMΩ for JFET and 10^9–$10^{15}\Omega$ for MOSFET.

→ FET is less noise than BJT.

→ FET is less effect by radiation.

→ FET's are more thermally stable than BJT.

→ FET occupies less space than BJT hence they have preferred in integrated circuits.

→ FET has smaller size, high Efficiency and long life

→ FET has very high power gain.

→ FET is a voltage control device since most of the signals to be processed are voltage signals. Hence FET are better than BJT.

→ FET is a three terminal device. The three terminal are source, gate and drain.

→ In practically 4th terminal is there ie channel or Substrate.

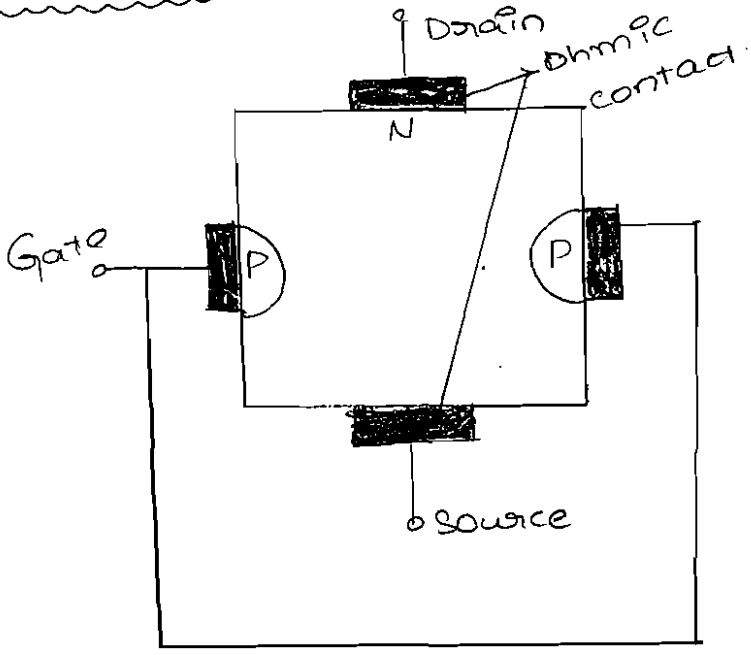
→ We know that in a BJT the o/p current I_C is controlled by base current I_B hence BJT is a current control device.

→ In feet the voltage b/w gate and source (V_{GS}) controlls the drain current I_D. Hence FET is a voltage controlled device.

→ The name field effect is derive from the o/p current flow is controlled by an electric field setup in the device by an externally applied voltage b/w gate and source terminals.

→ In FET current is carried by only one type of charge carriers either electrons or holes hence FET is called uni polar Devices.

Construction of n-channel JFET And Symbol.



N-channel JFET

→ The basic construction of N-channel JFET is as shown in fig(a).

→ It consists of an N-type sc substrate (here substrate is very lightly doped which is called channel) is taken and at its two ends two ohmic contacts are made which are the drain & source terminals of the FET.

→ Two P-type heavily doped region diffused on opposite sides of lightly channel region thus 2 P-type regions form 2 PN junctions the space blw the junctions is called channel.

→ Both the P-type regions are connected internally through a single wire ie called Gate.

* Source:

→ It is a terminal to which the majority carriers enters the bar.

* Drain:

→ It is a terminal through the which the majority carriers leaves the bar.

Gate:

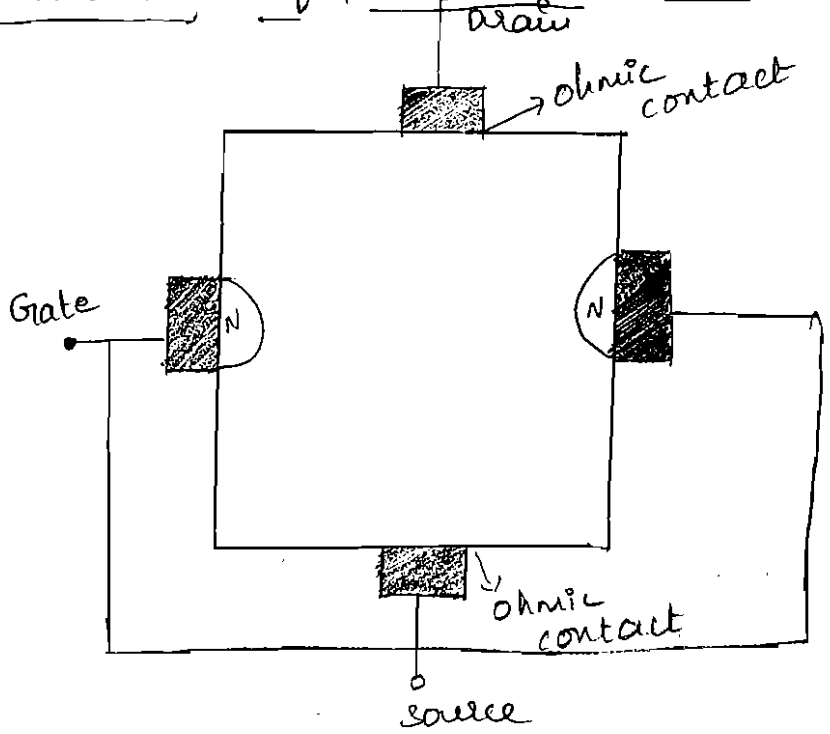
→ The 2 heavily doped regions connected to a common terminal is called Gate."

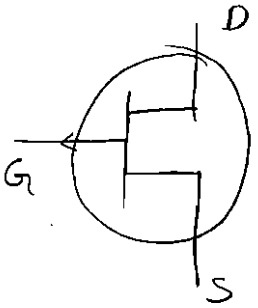
→ It is used to control the flow of current from source to Drain.

* Channel & Substrate :-

→ The region of n-type or p-type material b/w 2 heavily doped regions is the channel through which the majority charge carriers moves from source to Drain.

* Construction of p-channel JFET and Symbol





Symbol of pchannel JFET

P-channel JFET

→ The basic construction of p-channel JFET is as shown in fig(a).

→ It consists of an p-type sc substrate (here substrate is very lightly doped which is called

channel) is taken and at it its two ends two ohmic contacts are made which are the drain & source terminals of the FET.

→ Two N-type heavily doped region diffused on opposite sides of lightly doped region thus 2 n-type regions form 2 pn junctions the space blw the junctions is called channel.

→ Both the p-type regions are connected internally through a single wire ie called Gate

*Source:

→ It is a terminal to which the majority carriers enters the ball.

*Drain:

→ It is a terminal to which the majority carriers leaves the ball.

*Gate:

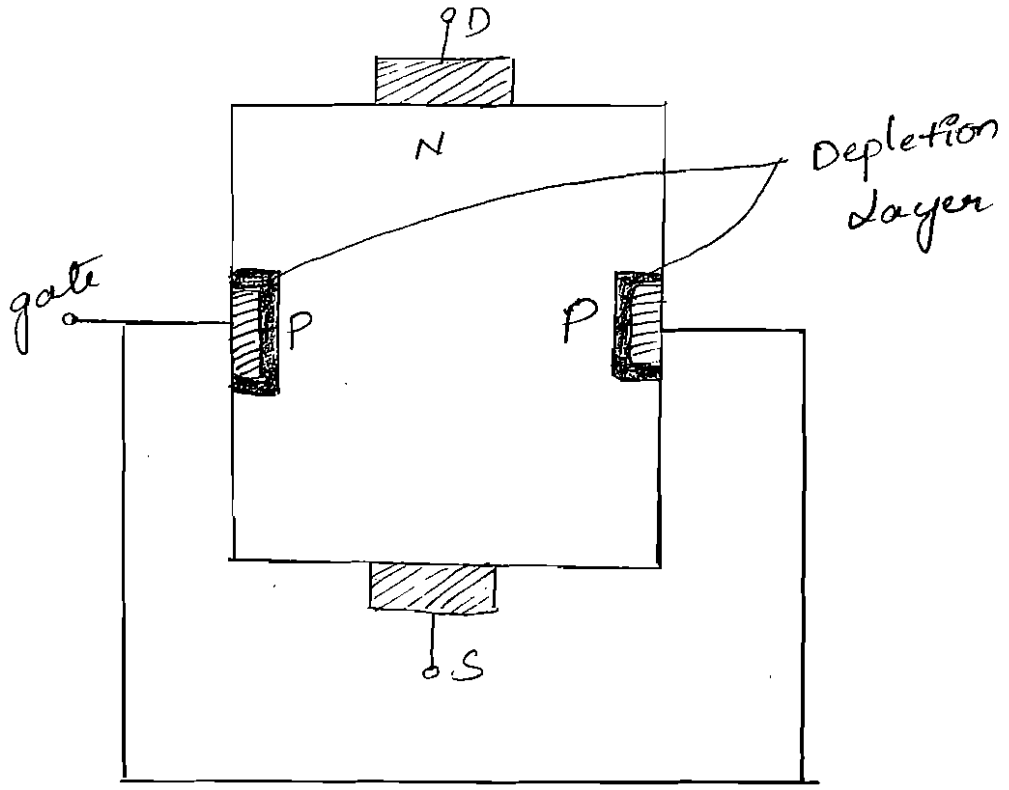
→ The 2 heavily doped regions connected to a common terminal is called "Gate".

→ It is used to control the flow of current from source to Drain.

*Channel

The region of n-ptype & p-type material blw 2 heavily doped region it is channel through

Operation of N-Channel JFET



fig(a): Construction of n-channel JFET

case (i)

When $V_{GS}=0$ and $V_{DS}=0$.

→ When no voltage b/w Drain and source, and Gate and source the thickness of depletion region around the pn junction is uniform as shown in fig(a).

case (ii)

When $V_{DS}=0$ and V_{GS} decreased from zero(0).

→ In this the pn junctions are reverse biased hence the thickness of depletion region increases as V_{GS} decreased from zero.

→ The reverse bias voltage across the pn junction is increased hence the thickness of the depletion region in the channel increases until the 2 depletion regions make contact with each other.

→ In this condition the channel is said to be cut-off the value of V_{GS} which is required to cutt off the channel is called cutt off voltage (V_p).

Case(iii)

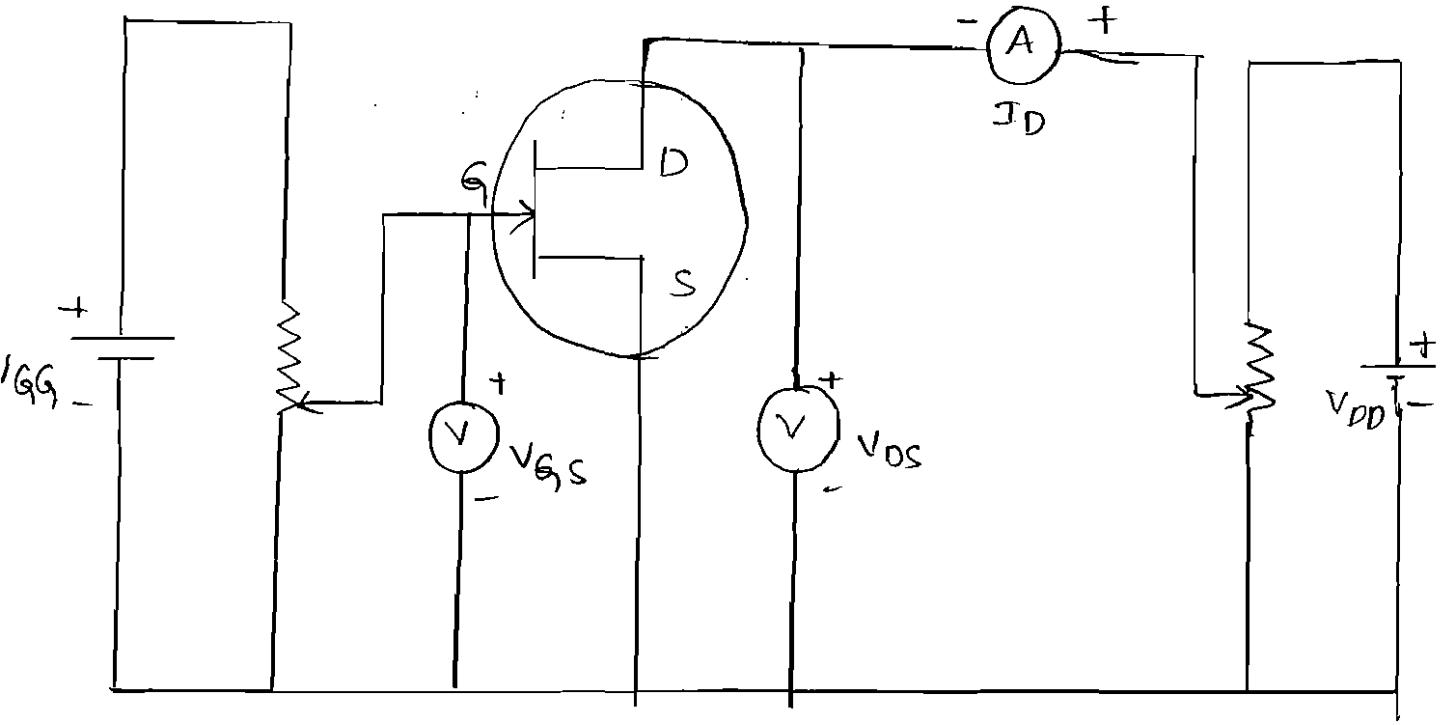
When V_{DS} & V_{GS} are applied.

→ The channel is established blw source & Drain the current flows from source to Drain i.e the drain current (I_D).

JFET CHARACTERISTICS (Mid)

or

N-channel Characteristics



They are 2 types of characteristics

1. Drain or o/p characteristics
2. Transfer characteristics

Drain or o/p characteristics

A curve drawn blw drain current I_D and drain to source voltage V_{DS} of FET at constant Gate to source voltage V_{GS} is known as Drain characteristics of FET.

Drain characteristics are divided into 3 regions.

1. ohmic region
2. Saturation or pinch-off region.
3. Breakdown region

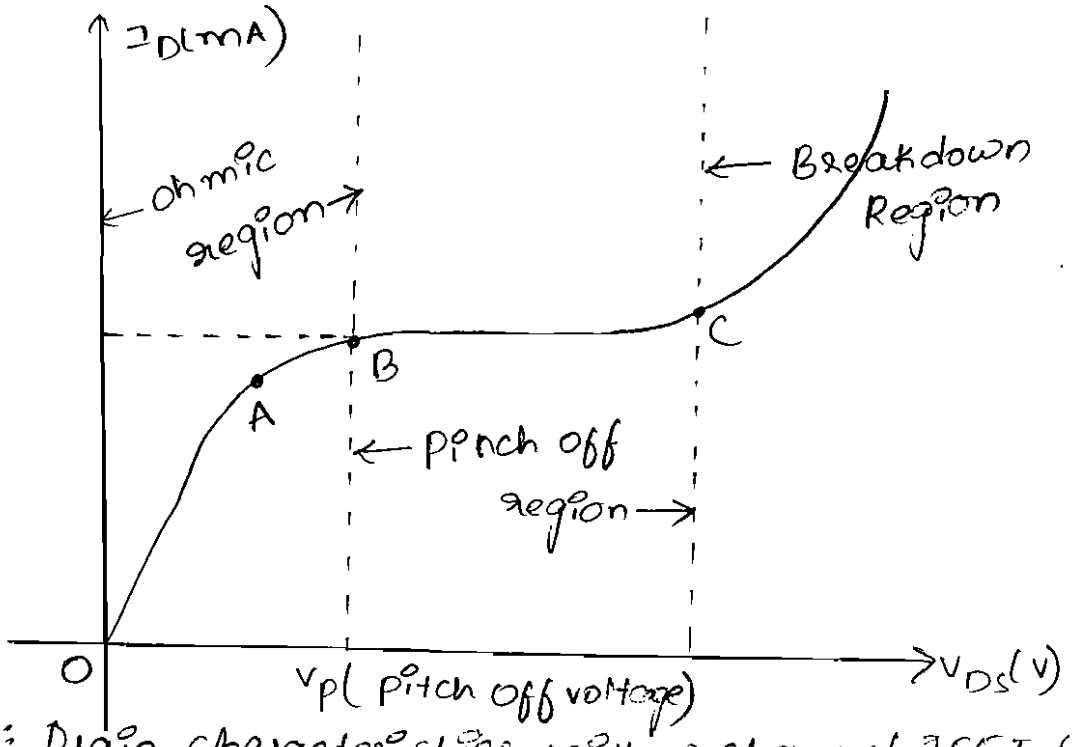
Case (i) → ohmic region

(a) When $V_{GS}=0$ and $V_{DS}=0$

When $V_{GS}=0$ the channel is entirely open but $V_{DS}=0$ so there is no attractive force for the majority carriers and hence drain current does not flow

$I_D=0$

(b) When $V_{GS}=0$ and $V_{DS}>0$



fig(b): Drain characteristics with n-channel JFET with $V_{GS}=0$

→ As V_{DS} is increased the electrons start flowing from source to Drain terminals to a channel b/w depletion layers and Drain current I_D increases linearly upto a point ie knee point.

→ The voltage corresponding to the knee point is known as pitch of voltage and it is denoted by V_p.

→ This shows that FET behave like an ordinary resistor till knee point. The region from $V_{DS}=0V$ to V_{DS} peak voltage is called ohmic region.

→ The FET resistance in the ohmic region is given by $V_{DS} \simeq I_D \cdot R_{DS}$

$$R_{DS} \simeq \frac{V_{DS}}{I_D}$$

$$\boxed{R_{DS} \simeq \frac{V_P}{I_{DSS}}}$$

Where V_p = pitch off voltage

I_{DSS} = maximum Drain current.

* Pitch-off or Saturation Reagion 20/9/16

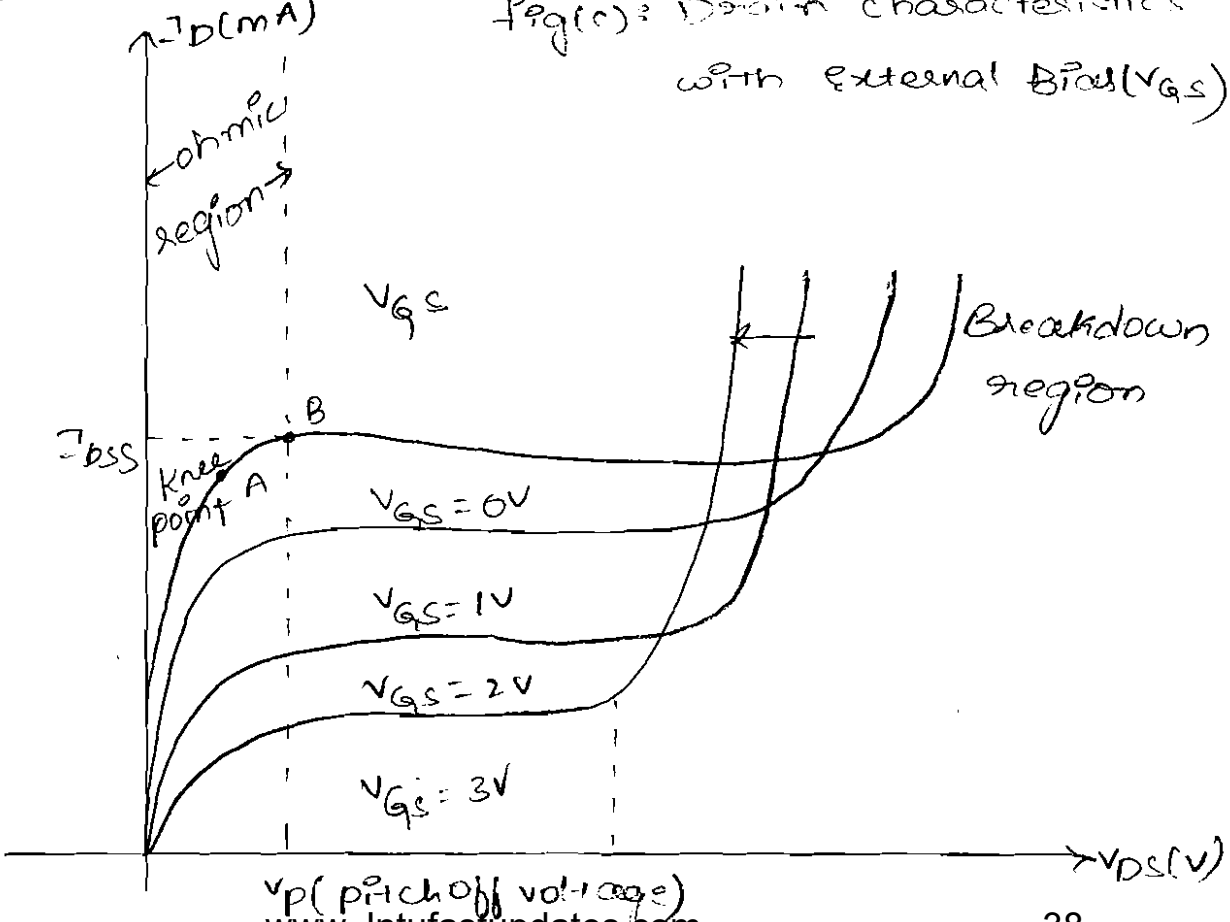
→ As V_{DS} is further increased the channel resistance is also increases in such a way that I_D practically remains constant upto a point c the reagion B to C is called pinch off & saturation region.

→ In this region a FET operates as a constant current device and drain current is related to gate voltage by $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

where I_{DSS} = Drain Saturation Current when gate & source is shorten.

This above Equation is known as Shockley. The pitch off region normal operating reagion as JFET when used as an amplifier.

Breakd



fig(c): Drain characteristics with external Bias(V_{GS})

Breakdown Region

With increase of continuous V_{DS} corresponding to point C called Avalanche breakdown voltage.

→ Breakdown occurs the gate junction takes place the current I_D.

→ This happens because of the reverse biased pn junction undergoes Avalanche breakdown varying a small change in V_{GS} producing a very large current I_D.

case(ii)

(Refer back for diagram)

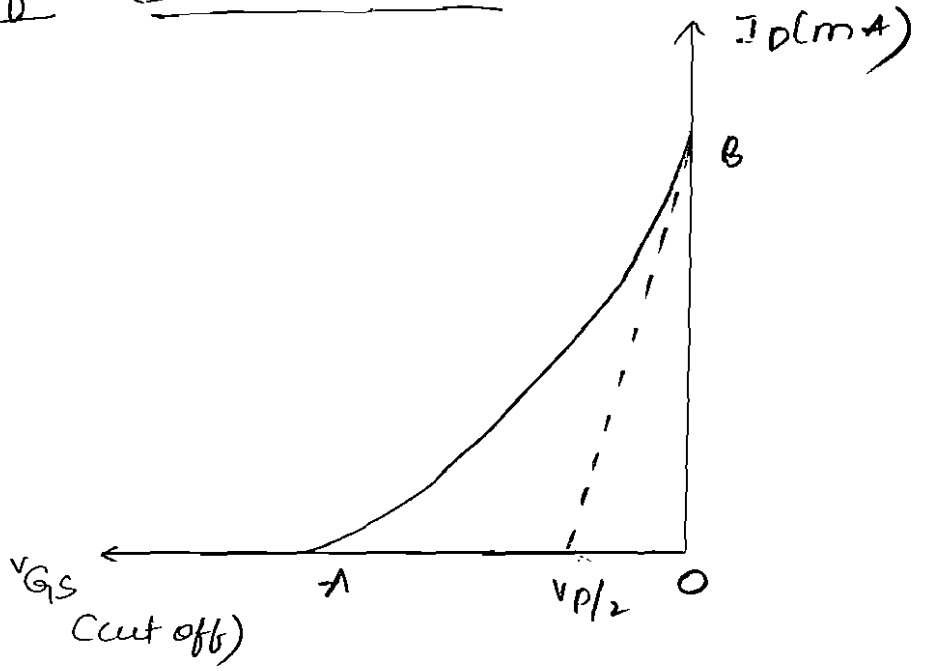
Drain Characteristics with External bias (V_{GS})

→ It is seen that as the -ve gate biased voltage increased the resulting I_D vs V_{DS} curve are similar to $V_{GS} = 0V$ except for the following points.

i) The Avalance Breakdown occurs at lower values of V_{DS} the reason is that the reverse bias gate voltage adds to the drain voltage there by increasing the voltage Effect across at the junction.

ii) The maximum saturation drain current reduces as the -ve bias voltage increases.

Transfer Characteristics



fig(d) Transfer

→ The TC a plot of drain current (I_D) Vs gate to source voltage (V_{GS}). For a constant value voltage blw drain to source.

The relationship blw the drain current (I_D) as gate to source voltage is non-linear.

→ The relationship is defined by Shockleys eqn is given by

$$I_D \simeq I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\left[1 - \frac{V_{GS}}{V_P}\right]^2 = \frac{I_D}{I_{DSS}}$$

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$1 - \sqrt{\frac{I_D}{I_{DSS}}} = \frac{V_{GS}}{V_P}$$

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

JFET PARAMETERS

1. Drain to source Resistance (r_d).

→ It is defined as the ratio of change in drain to source voltage to the change in drain current at constant gate to source voltage

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}=\text{constant}}$$

* r_d is very large from 10KΩ - 100MΩ

2. Trans Conductance (g_m)

→ It is defined as the ratio of change in drain current to change in gate to source voltage at constant drain to source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=\text{constant}}$$

We know that

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \longrightarrow (1)$$

partially differentiate Equ(1) w.r to V_{GS}

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS} \cdot 2\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{-1}{V_P}\right]$$

$$= -\frac{I_{DSS}}{V_P} \cdot 2\left[1 - \frac{V_{GS}}{V_P}\right] \longrightarrow (2)$$

from Eqn (1) $1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \longrightarrow (3)$

Substitute Eqn (3) in Eqn (2)

$$= -\frac{I_{DSS}}{V_P} \cdot 2 \cdot \sqrt{\frac{I_D}{I_{DSS}}}$$

$$= -\frac{2 I_{DSS}}{V_P} \cdot \frac{\sqrt{I_D}}{\sqrt{I_{DSS}}}$$

$$= -\frac{2\sqrt{I_{DSS}} \cdot \cancel{\sqrt{I_{DSS}}}}{V_P} \cdot \frac{\sqrt{I_D}}{\cancel{\sqrt{I_{DSS}}}}$$

$$\boxed{g_m = \frac{-2\sqrt{I_{DSS} \cdot I_D}}{V_P}}$$

ie Trans conductance

Let $g_m = g_{mo}$, when $V_{GS} = 0$.

from Eqn (6)

$$I_D = I_{DSS}$$

$$\boxed{g_{mo} = \frac{-2 \cdot I_{DSS}}{V_P}}$$

where g_{mo} indicates the trans conductance when $V_{GS} = 0$.

$$\therefore g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

The conductance g_m is also called as Mutual conductance. g_m ranges from 150μV to 250μV.

Amplification factor (μ)

→ It is defined as the ratio of change in Drain to source voltage to change in gate to source voltage at constant drain current.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Bigg|_{I_D = \text{constant}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \mu = r_d \cdot g_m$$

Problems

1. For a silicon $\alpha = 0.995$ and emitter current is 10mA and leakage current $I_{CO} = 0.5mA$. Find I_C, I_B, β, I_{CEO}.

2. Derive the relation b/w α and β given $I_E = 2.5mA$, $\alpha = 0.98$ and $I_{CBO} = 10\mu A$. Calculate I_B and I_C.

* MOSFET (Metal Oxide SC

→ It is a 3 terminal device the 3 terminals are 1. Source
2. Drain
3. Gate.

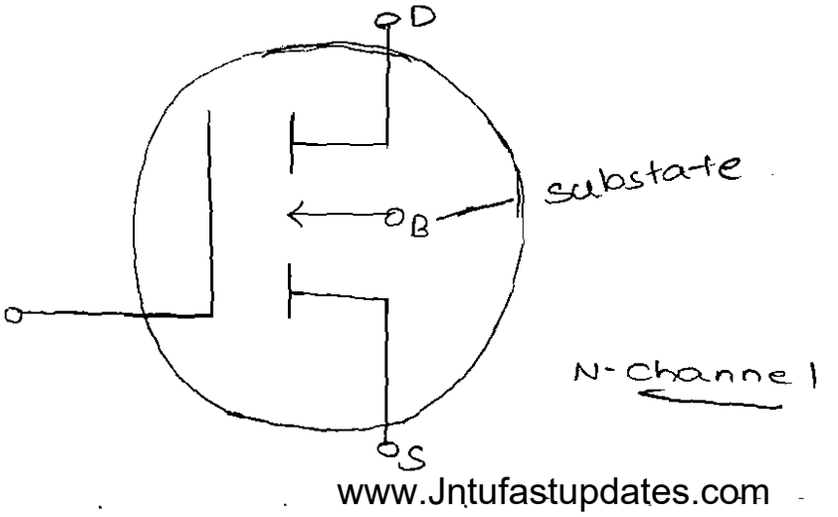
→ In MOSFET gate is insulated from channel sometimes called as Insulated gate fieldeffect transistor.

1. Enhacement MOSFET
   i) N-Channel Enhancement MOSFET.
   ii) P-Channel. " "

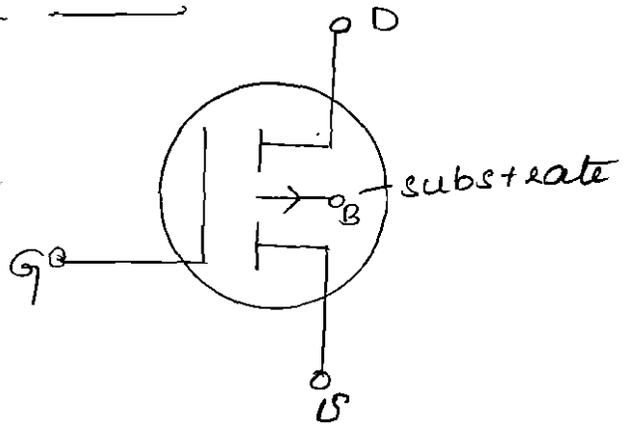
2. Depletion MOSFET
   i) N-Channel Depletion MOSFET.
   ii) P-channel " "

1. Enhancement MOSFET

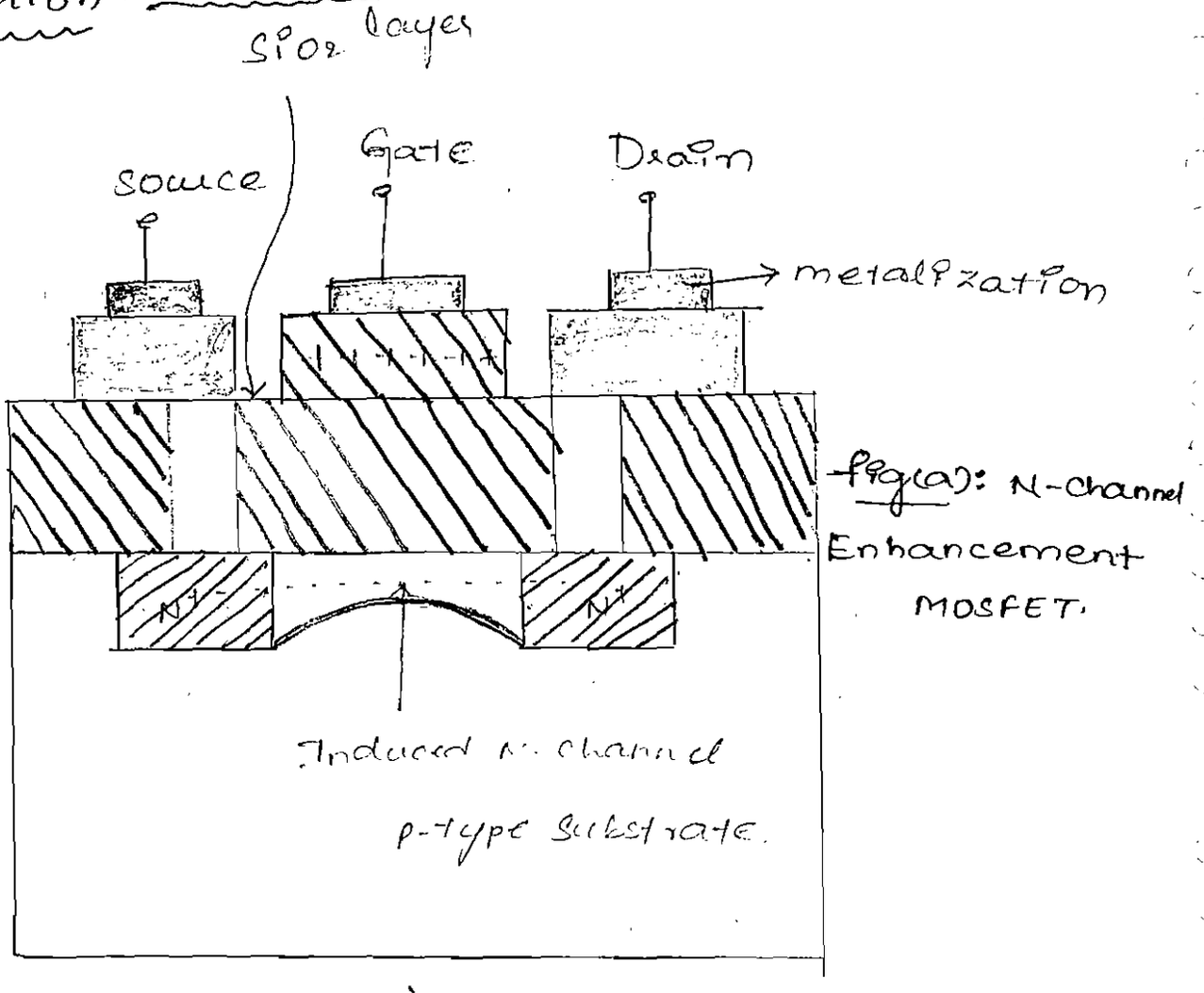
i) N-Channel Enhancement MOSFET



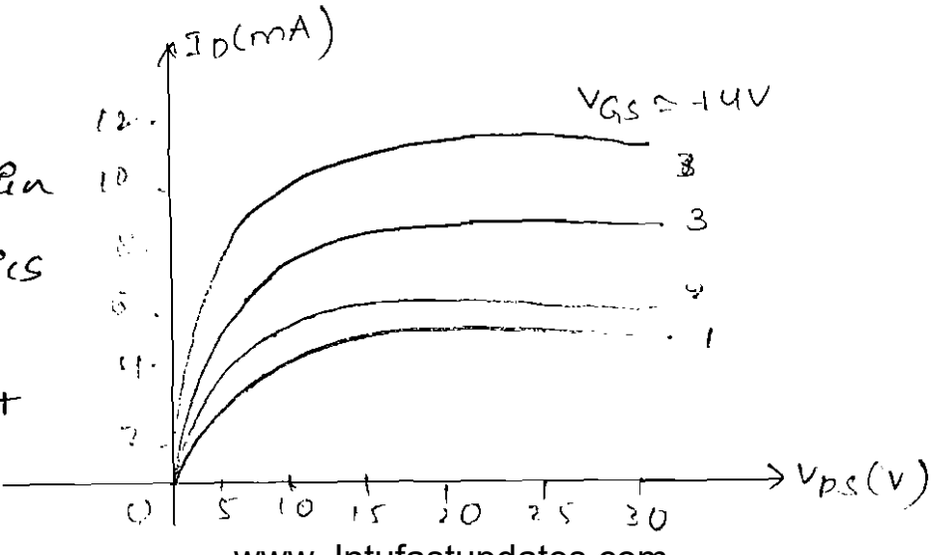
(ii) P-channel



Construction N-channel



fig(a): N-channel Enhancement MOSFET.



fig(b): Drain Characteristics of N-channel Enhancement MOSFET.

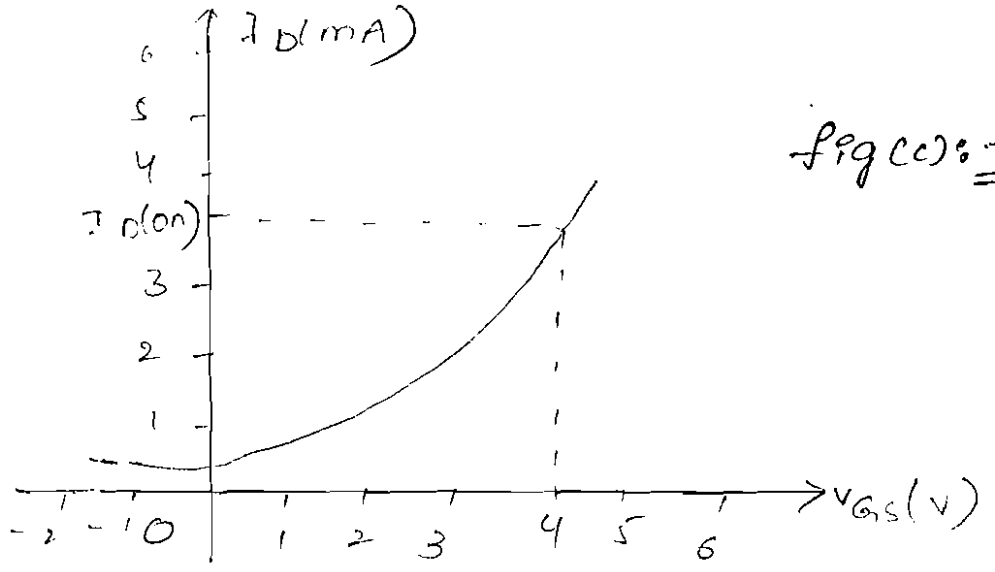


fig (c): TC

→ As there is no continuous channel in Enhancement MOSFET. This condition is represented by broken lines in the symbols to highly doped N^+ region are diffused in a lightly doped substrate.

⇒ One N^+ region is called source another one is called Drain.

→ A thin insulating layer of SiO_2 grown over the surface of the structure

→ Holes are coming cut in to the oxide layer allowing contact with source and Drain.

→ A thin layer of metal Aluminium is formed over the layer of SiO_2 this metal layer covers the Entire Channel region. It forms the gate G.

→ The metal area of the gate conjunction with the forms an a layer as shown in fig a. As the +ve voltage on the gate induces -ve charge in the SCR hence the conductivity of and I flows from the source to Drain through the induced channel thus the Drain current is Enhanced by the +ve gate v and the name Enhancement MOSFET